Designing a Single Socket Solution for AMD's Am29F080 and Intel's 28F008SA

Application Note

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AMD is delivering an 8 Megabit Flash memory that is pin and function equivalent to Intel's 28F008SA device in both the 40 pin TSOP and 44 pin PSOP packages. This application note will cover the details necessary to design a single socket that accommodates both devices.

PACKAGE CONSIDERATIONS

40-Pin TSOP

As noted in Figure 1 below the pinouts for AMD's Am29F080 and Intel's 28F008SA are virtually identical. The only exception being pin 11 that is V_{PP} on the 28F008SA device and is a No Connect (NC: no internal connection) on the Am29F080.

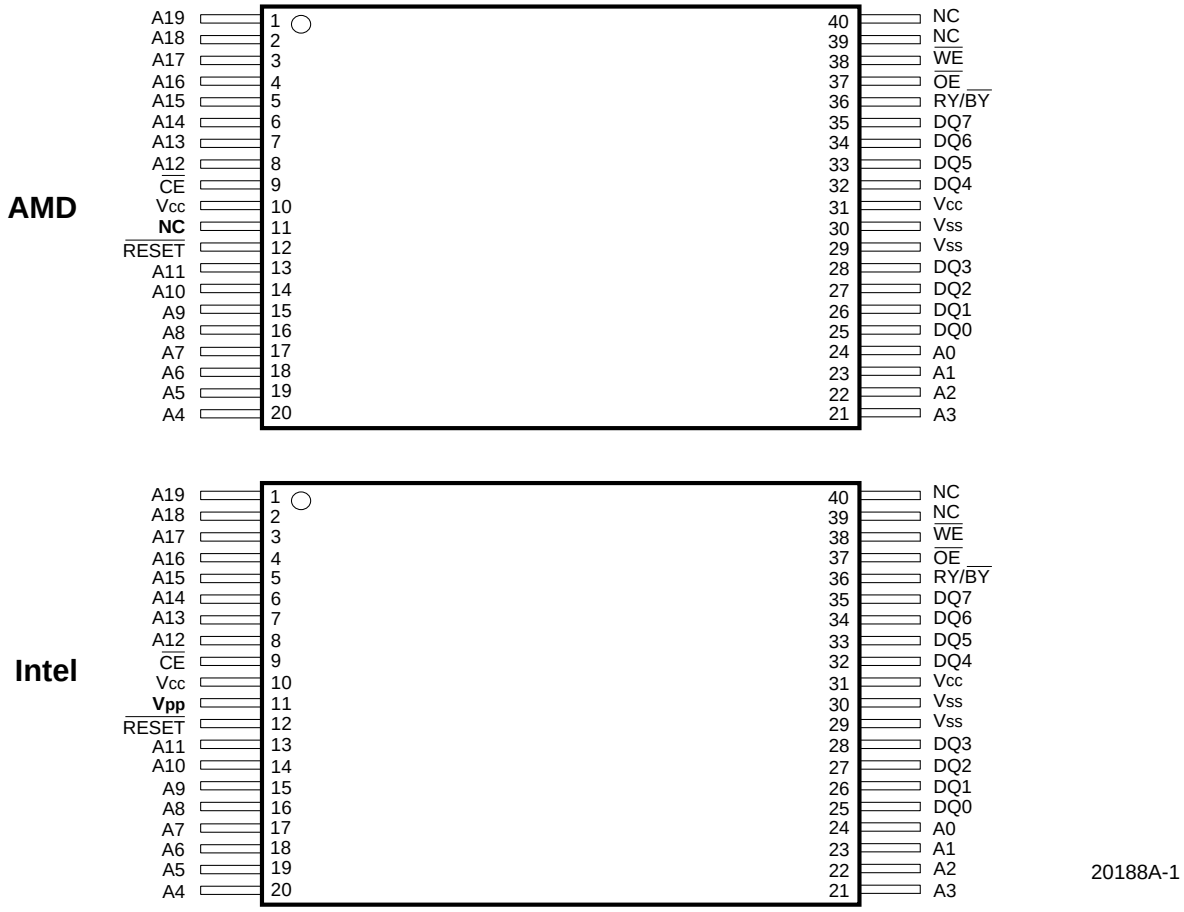

Figure 1. Pinout Comparison between AMD's Am29F080 and Intel's 28F008SA in 40 Pin TSOP Package

44-Pin PSOP

As noted in Figure 2 below the pinouts for AMD's Am29F080 and Intel's 28F008SA are virtually identical. The only exception being pin 1 that is V_{PP} on the 28F008SA device and is a No Connect (NC: no internal connection) on the Am29F080.

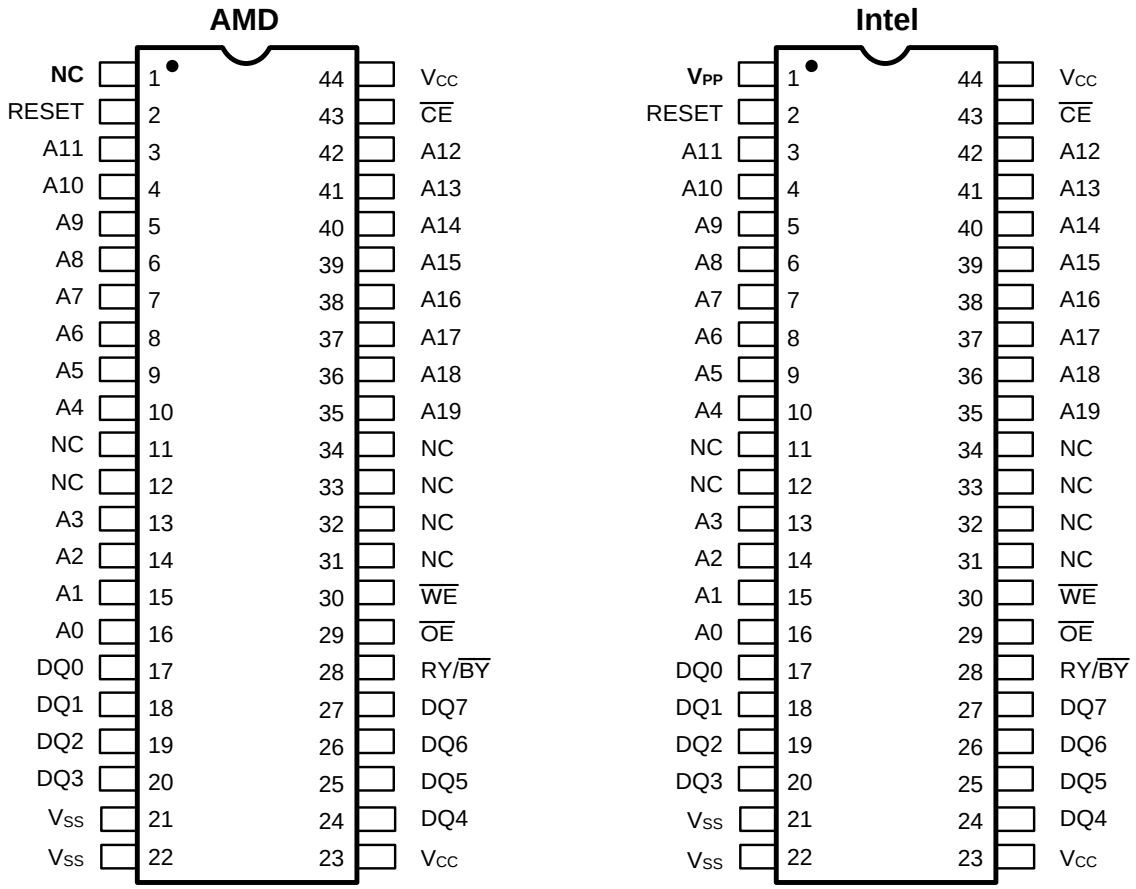

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Figure 2. Pinout Comparison between AMD's Am29F080 and Intel's 28F008SA in 44 Pin PSOP Package

HARDWARE DESIGN ISSUES

Because the devices are pin compatible in all respects, except for pin 11 in the TSOP and pin 1 in the PSOP packages, complex changes are not required. Simply enabling (28F008SA) or disabling (Am29F080) the V_{PP} pin will make the system hardware compatible with either manufacturers' device in either package.

SYSTEM SOFTWARE DESIGN

There are some fundamental differences in the devices from a power management and software implementation perspective. The following sections detail differences manifested in the software required to utilize specific device features. Assuming the system requires support for both devices, these differences may easily be arbitrated with the implementation of a software decision tree embedded in the system software. The decision tree chooses the correct manufacturer's device driver (software) by reading each manufacturer's specific device identification bits. AMD provides a prewritten version of the Am29F080 software driver; it is available on the CSE BBS under the NVD directory.

Standby Power Consumption

Both devices will go into the standby mode using TTL voltage levels. However, to maximize the powerdown features, the devices need to react to CMOS voltage levels or use the Reset/Powerdown ($\overline{RP}$) pin.

Table 1. Power Consumption Comparisons

TTL Level Inputs	CMOS Level Inputs	Reset pin induced
$\overline{CE} = \overline{RP} = V_{IH}$	$\overline{CE} = \overline{RP} = V_{CC} + 0.2$ V	$\overline{RP} = V_{IL}$ or nominal 0.0 V
AMD: 1.0 mA max	AMD: 5.0 µA max	AMD: 5.0 µA max
Intel: 2.0 mA max	Intel: 100 µA max	Intel: 1.2 µA max

Note:

1. These are maximum values, typical values can be much less, refer to each manufacturer's data sheet for their typical estimates.

Reset Pin Differences

Intel and AMD's use of the Reset/Powerdown Pin ($\overline{RP}$) is different for various reasons.

AMD uses $\overline{RP}$ active low as a hardware tie to the system CPU reset circuitry. This feature enables firmware stored in the Flash device to reboot the system after receipt of a Reset command from the CPU. The Am29F080 requires a 500 ns latency period after $\overline{RP}$ goes high and it must be incurred prior to a read or other valid operation attempt. The 20 µs specification is the maximum time the Flash device takes, after receipt of a Reset command, before it can aid CPU reboot of the system. The Am29Fxxx family does not use an external V_{PP} voltage; therefore $\overline{RP}$ control is not necessary for prevention of inadvertent writes during power transitions.

The Am29F080 also has a low power, CMOS level standby mode, I_{CC4} (5 µA max), induced with $\overline{RP}$ active low. However, I_{CC4} does not provide any additional power savings over the $\overline{CE}$ controlled standby mode, I_{CC3} (i.e. $I_{CC4} = I_{CC3}$). $\overline{RP}$ induced powerdown does require a 500 ns latency period after going high before a read or other valid operation attempt. But, exiting I_{CC3} *does not* require any latency period for continued Flash operations.

Intel uses the $\overline{RP}$ to put their device into a deep powerdown mode (1.2 µA max through V_{CC}). Intel also has a V_{PP} standby component that must be considered when V_{PP} is on and the device is put into standby. V_{PP} standby can be a maximun of 15.0 µA when $\overline{CE}$ controlled (and $V_{PP} < V_{CC}$) or as much as 5.0 µA when standby is induced by $\overline{RP}$ low.

Intel can also use the $\overline{RP}$ control for two additional purposes. One is a preventive measure in blocking inadvertent writes that may occur during V_{PP} power transitions. The second may be as a hardware reset mechanism when the device is tied to the system reset circuitry. A delay of 400 ns is required anytime $\overline{RP}$ transitions from low to high and it must be incurred prior to a read or other valid operation attempt. Intel does not specify a minimum $\overline{RP}$ pulse width.

RY/$\overline{BY}$ Pin Implementation

Both manufacturers use a RY/$\overline{BY}$ pin. The table below details its primary functionality. However, a check of Intel's RY/$\overline{BY}$ pin may be required as part of the software required to accurately determine the status of a program or erase operation.

Table 2. RY/$\overline{BY}$ Pin Comparison

Pin Condition	AMD	Intel
$RY/\overline{BY} = V_{IH}$	– Device is ready to accept new commands – Block Erase is suspended	– Device is ready to accept new commands – Sector Erase is suspended
$RY/\overline{BY} = V_{IL}$	– Sector Erase or program is in progress – Device will accept Erase Suspend command only – Device is in I_{CC4}	– Block Erase or program is in progress – Device will accept Erase Suspend command only – Device is in Deep Powerdown

Table 3. Status Bit Comparison Chart

I/O Bit	AMD	Intel
DQ7	Embedded Algorithms in Progress	Write State Machine Status
DQ6	Toggle Bit for Program/Erase Status	Erase Suspend Status
DQ5	Exceeded Time Limits	Block Erase Suspended
DQ4	Reserved	Byte Write Status
DQ3	Sector Erase Timer	V_{PP} Status
DQ2	Erase/Erase Suspend Operation Active	Reserved
DQ1	Reserved	Reserved
DQ0	Reserved	Reserved

Device Operation Status

Both manufacturers provide methods for the system CPU to determine the state of the Flash device at any given time. Both devices provide this data after specified address and data commands are written to the device. These address and data commands are detailed in the respective device data sheets. A summary of the differences is listed above. Once again, it must be noted these differences are accommodated with device software drivers tailored for each device and invoked via a software decision tree.

Data Protection

Both manufacturers employ multiple methods to guard against inadvertent writes to the Flash device. Their respective methods are quite different and require attention to detail when installing the devices into a system without benefit of a pre-written device driver. A summary of the methods and their differences follows:

Address/Data Command Sequences

AMD uses a 4 command write and 6 command erase address/data sequence to setup and execute write and erase operations. These longer command sequences and the absence of an external V_{PP} power supply are a primary connerstone of the Am29F080's inadvertent write protection. They are consistent throughout the entire Am29Fxxx family of devices.

Intel uses a 2 command sequence to initiate both erase and write operations. The first command is for operation setup and the second is for erase confirm or program data, whichever is appropriate. If V_{PP} is applied during this two command sequence (without using preventive measures described in Intel's data sheet and Application Note #AP 374), the device is susceptible to inadvertent writes.

V_{PP} Control

AMD—There is no external control needed because the device generates and controls V_{PP} internally.

Intel—Switching V_{PP} off with a FET or taking $\overline{RP}$ low eliminates the chance of inadvertent writes.

Low V_{CC} Write Inhibit

AMD —V_{LKO} is 3.2 V min. Voltage levels between V_{LKO} max and V_{CC} min must be controlled by the user with logical inhibit of the device control pins.

Intel—V_{LKO} = 2.0 V min. Caution must be used when V_{PP} is on and Vcc is < V_{CC} max and > V_{LKO}.