

The PowerPC™ RISC Family Microprocessors

In Brief . . .

The PowerPC architecture is derived from the IBM Performance Optimized with Enhanced RISC (POWER) architecture. The PowerPC architecture shares all of the benefits of the POWER architecture but is optimized for single-chip implementations. The architecture design emphasizes parallel instruction execution and high throughput and allows for exceptional floating-point performance. The PowerPC architecture is powerful today and is scalable from palmtops to mainframes.

	Page
PowerPC™ RISC Microprocessors	2.4-2
MPC601 RISC Microprocessor	2.4-2
MPC602 RISC Microprocessor	2.4-3
MPC603 RISC Microprocessor	2.4-3
MPC603e RISC Microprocessor	2.4-6
MPC604 RISC Microprocessor	2.4-9
MPC604e RISC Microprocessor	2.4-9
MPC620 RISC Microprocessor	2.4-13
MPC105 PCI Bridge/Memory Controller	2.4-15
MPC106 PCI Bridge/Memory Controller	2.4-16

PowerPC™ RISC Microprocessors

The PowerPC Architecture™, developed jointly by Motorola, IBM, and Apple, is based on the POWER Architecture™ implemented by the RISC System/6000™ family of computers. The PowerPC architecture takes advantage of recent technological advances in such areas as process technology, compiler design, and RISC (reduced instruction set computer) microprocessor design to provide software compatibility across a diverse family of implementations, primarily single-chip microprocessors, intended for a wide range of systems, including battery-powered personal computers, embedded controllers, high-end scientific and graphics workstations, and multiprocessing, microprocessor-based mainframes.

To provide a single architecture for such a broad assortment of processor environments, the PowerPC architecture is both flexible and scalable.

The flexibility of the PowerPC architecture offers many price/performance options. Designers can choose whether to implement architecturally-defined features in hardware or in software. For example, a processor designed for a high-end workstation has greater need for the performance gained from implementing floating-point normalization and denormalization in hardware than a battery-powered, general-purpose computer might.

The PowerPC architecture is scalable to take advantage of continuing technological advances — for example, the continued miniaturization of transistors makes it more feasible to implement more execution units and a richer set of optimizing features without being constrained by the architecture.

The PowerPC architecture defines the following features:

- Separate 32-entry register files for integer and floating-point instructions. The general-purpose registers (GPRs) hold source and target data for integer arithmetic instructions, and the floating-point registers (FPRs) hold source and target data for floating-point arithmetic instructions.
- Instructions for loading and storing data between the memory system and either the FPRs or GPRs.
- Uniform-length instructions to allow simplified instruction pipelining and parallel processing instruction dispatch mechanisms.
- Nondestructive use of registers for arithmetic instructions in which the second, third, and sometimes the fourth operand, typically specify source registers for calculations whose results are typically stored in the target register specified by the first operand.
- A precise exception model (with the option of treating floating-point exceptions imprecisely).
- Floating-point support that includes IEEE-754 floating-point operations.
- The ability to perform both single- and double-precision floating-point operations.

- A flexible architecture definition that allows certain features to be performed in either hardware or with assistance from implementation-specific software depending on the needs of the processor design.
- User-level instructions for explicitly storing, flushing, and invalidating data in the on-chip caches. The architecture also defines special instructions (cache block touch instructions) for speculatively loading data before it is needed, potentially reducing the effect of memory latency.
- Definition of a memory model that allows weakly-ordered memory accesses. This allows bus operations to be reordered dynamically, which improves overall performance and in particular reduces the effect of memory latency on instruction throughput.
- Support for separate instruction and data caches (Harvard architecture) and for unified caches.
- Support for both big- and little-endian addressing modes.
- Support for 64-bit addressing. The architecture supports both 32-bit or 64-bit implementations. This document typically describes the architecture in terms of the 64-bit implementations in those cases where the 32-bit subset can be easily deduced.

MPC601 RISC Microprocessor

The MPC601 is the first implementation of the PowerPC architecture. The MPC601 implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits. For 64-bit PowerPC implementations, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The MPC601 is a superscalar processor capable of issuing and retiring three instructions per clock, one to each of three execution units. Instructions can complete out of order for increased performance; however, the MPC601 makes execution appear sequential.

The MPC601 integrates three execution units — an integer unit (IU), a branch processing unit (BPU), and a floating-point unit (FPU). The ability to execute three instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for MPC601-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The MPC601 includes an on-chip, 32-Kbyte, eight-way set-associative, physically addressed, unified instruction and data cache and an on-chip memory management unit (MMU). The MMU contains a 256-entry, two-way set-associative, unified translation look-aside buffer (UTLB) and provides support for demand paged virtual memory address translation and variable-sized block translation. Both the UTLB and the cache use least recently used (LRU) replacement algorithms.

The MPC601 has a 64-bit data bus and a 32-bit address bus. The MPC601 interface protocol allows multiple masters to compete for system resources through a central external arbiter. Additionally, on-chip snooping logic maintains cache coherency in multiprocessor applications. The MPC601 supports single-beat and burst data transfers for memory accesses; it also supports both memory-mapped I/O and I/O controller interface addressing.

The MPC601 uses an advanced, 3.6-volts (601) or 2.5 volts (601v) CMOS process technology and maintains full interface compatibility with TTL devices.

Block Diagram

Figure 1 provides a block diagram of the MPC601 that illustrates how the execution units — IU, FPU, and BPU — operate independently and in parallel.

MPC602 RISC Microprocessor

The MPC602 is a low-cost, low-power implementation of the PowerPC RISC architecture. The MPC602 implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits. Floating-point operations involving either 32- or 64-bit data types in single-precision format are supported; however, floating-point operations involving 64-bit data types in double-precision format are not implemented in hardware and are instead trapped for emulation in software.

The MPC602 has four execution units—an integer unit (IU), a floating-point unit (FPU), a branch processing unit (BPU), and a load/store unit (LSU). The ability to execute four instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for MPC602-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined such that typically when the FPU pipeline is full, a single-precision instruction can complete every clock cycle.

The MPC602 provides dynamic and static power-saving modes. The three static modes — nap, doze, and sleep — progressively reduce the amount of power dissipated by the processor.

The MPC602 provides independent on-chip, 4-Kbyte, two-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). The MPC602 MMUs contain 32-entry, two-way set-associative, data and instruction translation lookaside buffers (DTLB and ITLB). The MPC602 provides an additional memory protection mechanism not defined by the PowerPC architecture. The 602's protection-only mode can control whether instructions can be fetched from 4-Kbyte instruction pages and whether data can be written to 4-Kbyte data pages.

The MPC602 has a single bus interface used for transferring both 32-bit addresses and either 32- or 64-bit data. This bus is time-multiplexed. The MPC602 interface protocol allows multiple masters to compete for system resources through a central external arbiter. The MPC602 provides a three-state coherency protocol that supports the modified, exclusive, and invalid (MEI) cache states. This protocol is a compatible subset of the MESI (modified/exclusive/shared/invalid) four-state protocol and operates coherently in systems that contain four-state caches.

The MPC602 uses an advanced, 3.3-V CMOS process technology and maintains full interface compatibility with TTL devices.

Block Diagram

The MPC602 block diagram in Figure 2 illustrates how the execution units — IU, FPU, BPU, and LSU — operate independently and in parallel.

MPC603 RISC Microprocessor

The MPC603 is the first low-power implementation of the PowerPC architecture. The MPC603 implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits. For 64-bit PowerPC implementations, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The MPC603 provides four software controllable power-saving modes. Three of the modes (the nap, doze, and sleep modes) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the MPC603 to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution or any external hardware.

The MPC603 is a superscalar processor capable of issuing and retiring a maximum of three instructions per clock. Instructions can execute out of order for increased performance; however, the MPC603 makes completion appear sequential.

The MPC603 integrates five execution units — an integer unit (IU), a floating-point unit (FPU), a branch processing unit (BPU), a load/store unit (LSU) and a system register unit (SRU). The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for MPC603-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

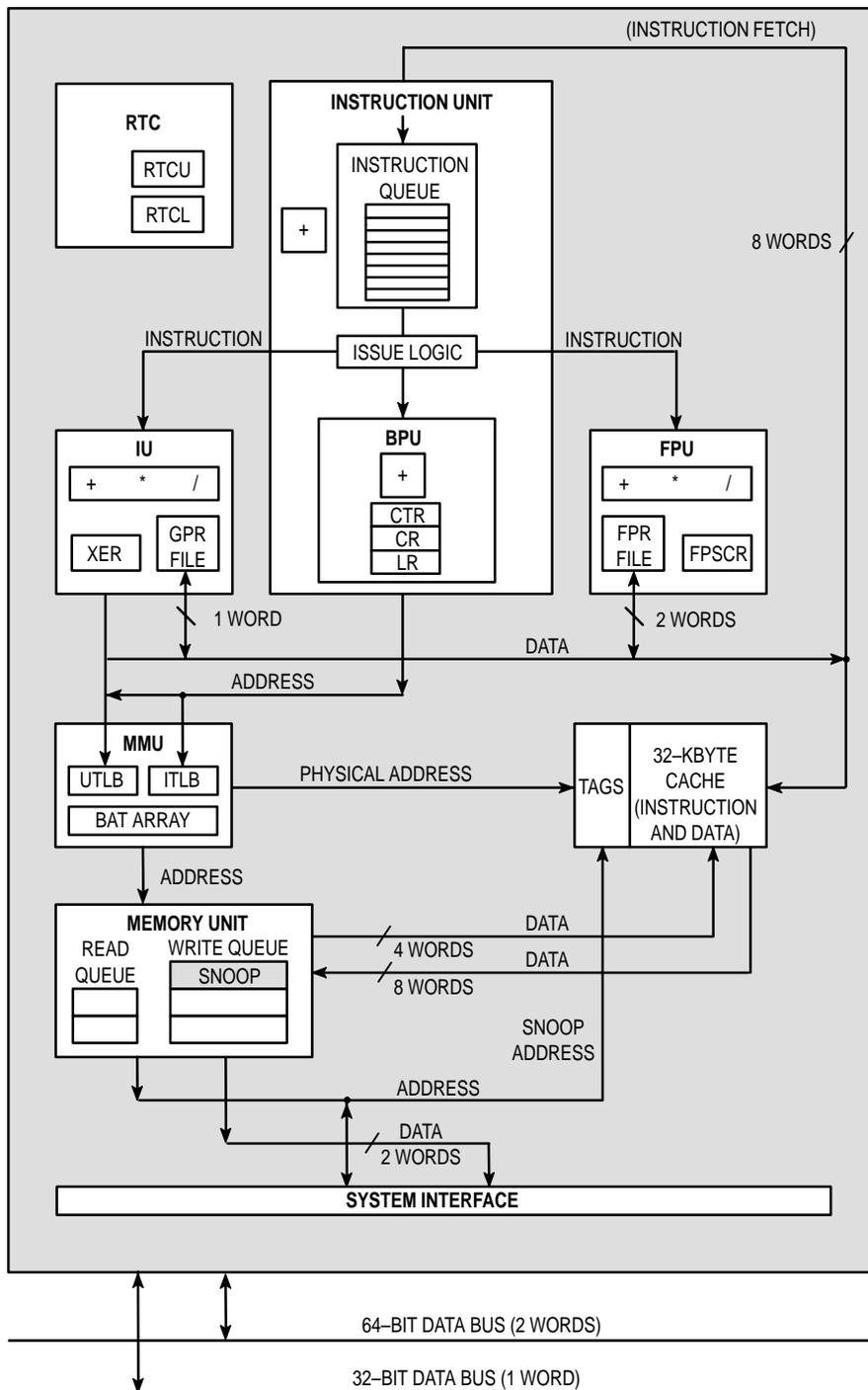


Figure 1. MPC601 Block Diagram

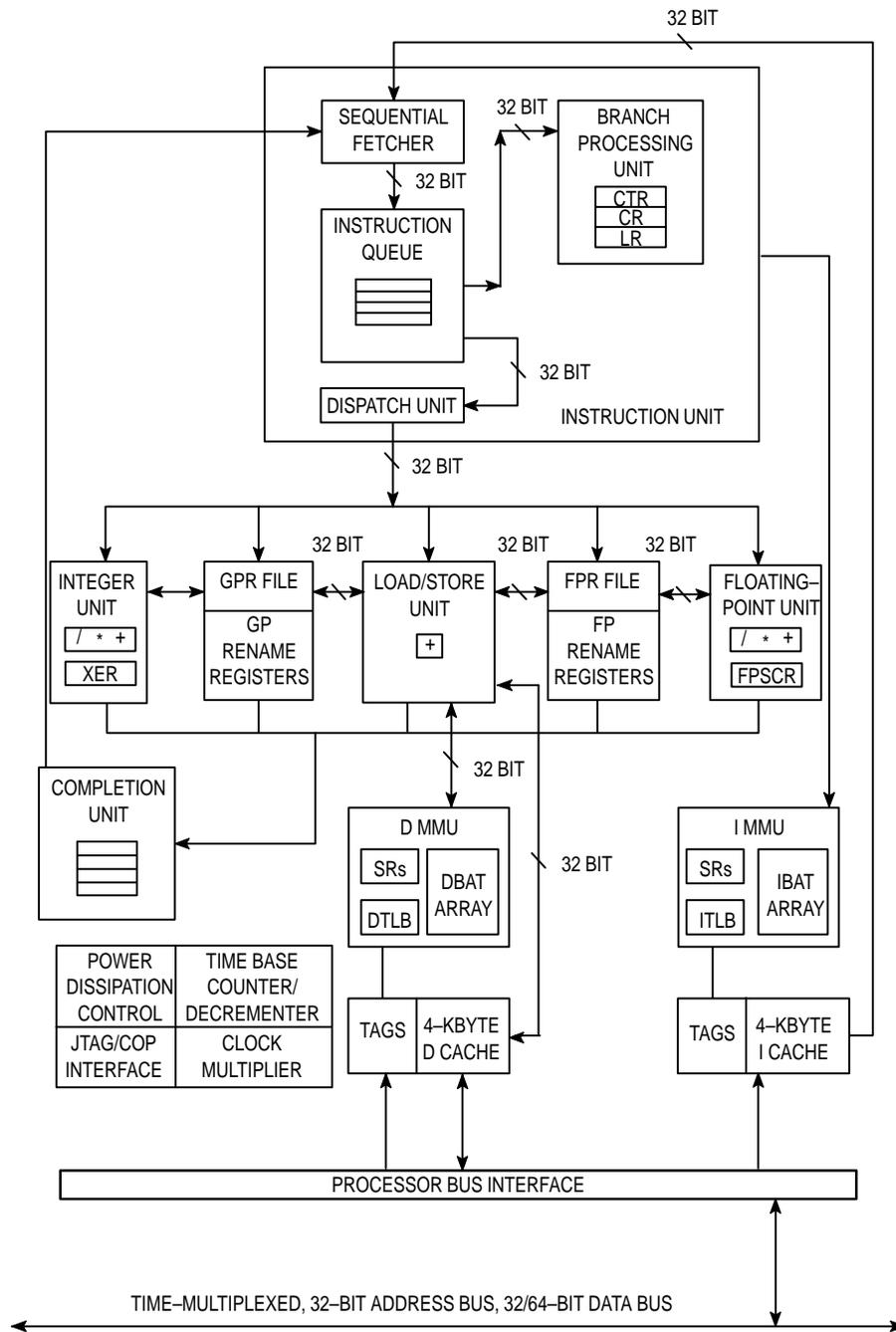


Figure 2. MPC602 Block Diagram

The MPC603 provides independent on-chip, 8-Kbyte, two-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation lookaside buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation.

The MPC603 has a selectable 32- or 64-bit data bus and a 32-bit address bus. The MPC603 interface protocol allows multiple masters to compete for system resources through a central external arbiter. The MPC603 provides a three-state coherency protocol that supports the Exclusive, Modified, and Invalid cache states. This protocol is a compatible subset of the MESI four-state protocol and operates coherently in systems that contain four-state caches. The MPC603 supports single-beat and burst data transfers for memory accesses; it also supports both memory-mapped I/O and I/O controller interface addressing.

The MPC603 uses an advanced, 3.3-V CMOS process technology and maintains full interface compatibility with TTL devices.

Block Diagram

Figure 3 provides a block diagram of the MPC603 that illustrates how the execution units — IU, FPU, BPU, LSU, and SRU — operate independently and in parallel.

The MPC603 provides address translation and protection facilities, including an ITLB, DTLB, and instruction and data BAT arrays. Instruction fetching and issuing is handled in the instruction unit. Translation of addresses for cache or external memory accesses are handled by the MMUs.

MPC603e RISC Microprocessor

The MPC603e is a low-power implementation of the PowerPC RISC architecture. The MPC603e implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits.

The MPC603e provides four software controllable power-saving modes. Three of the modes (the nap, doze, and sleep modes) are static in nature, and progressively reduce

the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the MPC603e to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The MPC603e is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can execute out of order for increased performance; however, the MPC603e makes completion appear sequential.

The MPC603e integrates five execution units — an integer unit (IU), a floating-point unit (FPU), a branch processing unit (BPU), a load/store unit (LSU), and a system register unit (SRU). The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for MPC603e-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The MPC603e provides independent on-chip, 16-Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation lookaside buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation.

The MPC603e has a selectable 32- or 64-bit data bus and a 32-bit address bus. The MPC603e interface protocol allows multiple masters to compete for system resources through a central external arbiter. The MPC603e provides a three-state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol is a compatible subset of the MESI (modified/exclusive/shared/invalid) four-state protocol and operates coherently in systems that contain four-state caches. The MPC603e supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/O accesses.

The MPC603e uses an advanced CMOS process technology and maintains full interface compatibility with TTL devices. The MPC603e is implemented in both a 2.5-V version (PID7V-603e) and a 3.3-V version (PID6-603e).

Block Diagram

Figure 4 provides a block diagram of the MPC603e that illustrates how the execution units — IU, FPU, BPU, LSU, and SRU — operate independently and in parallel.

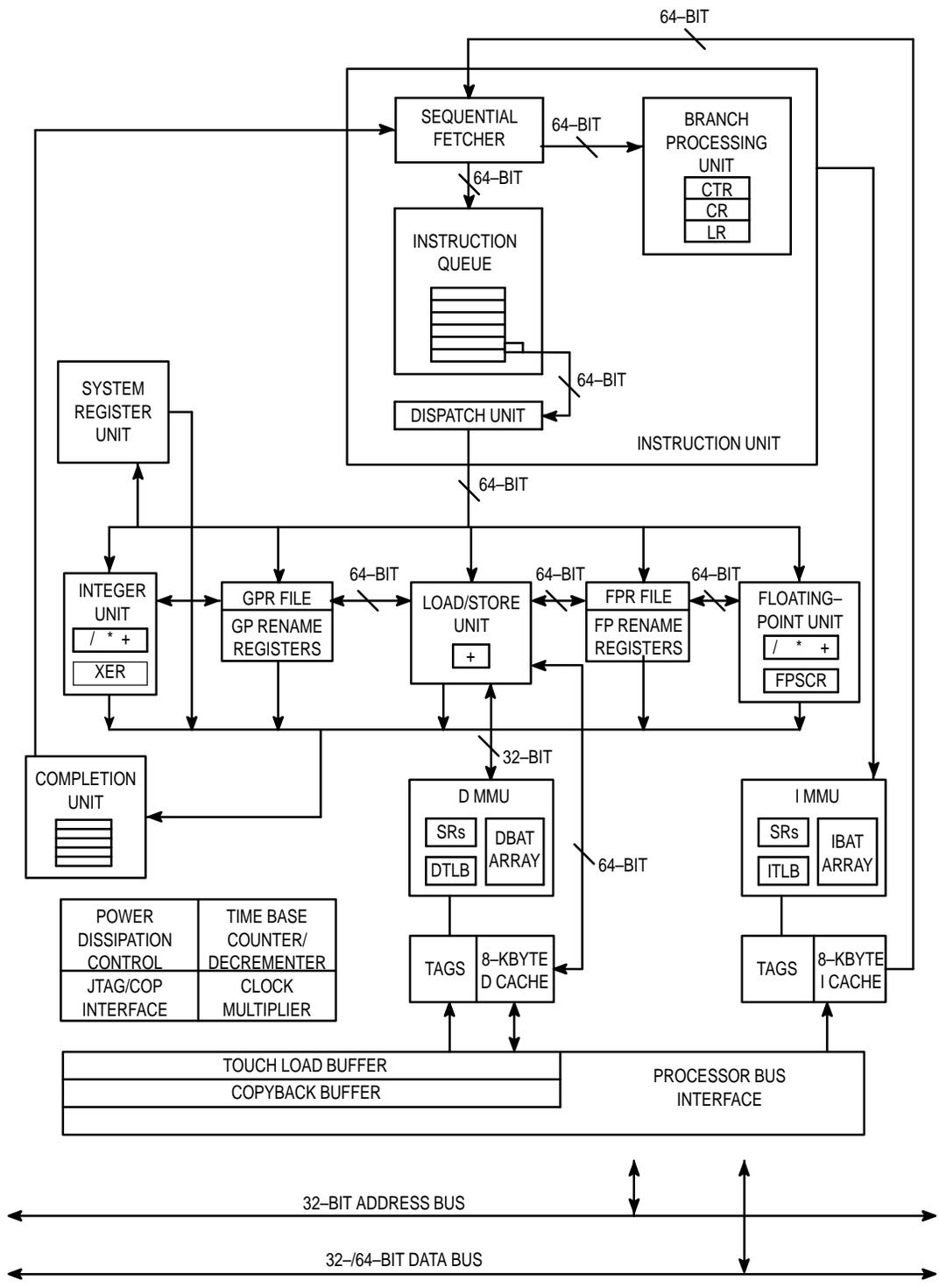


Figure 3. MPC603 Block Diagram

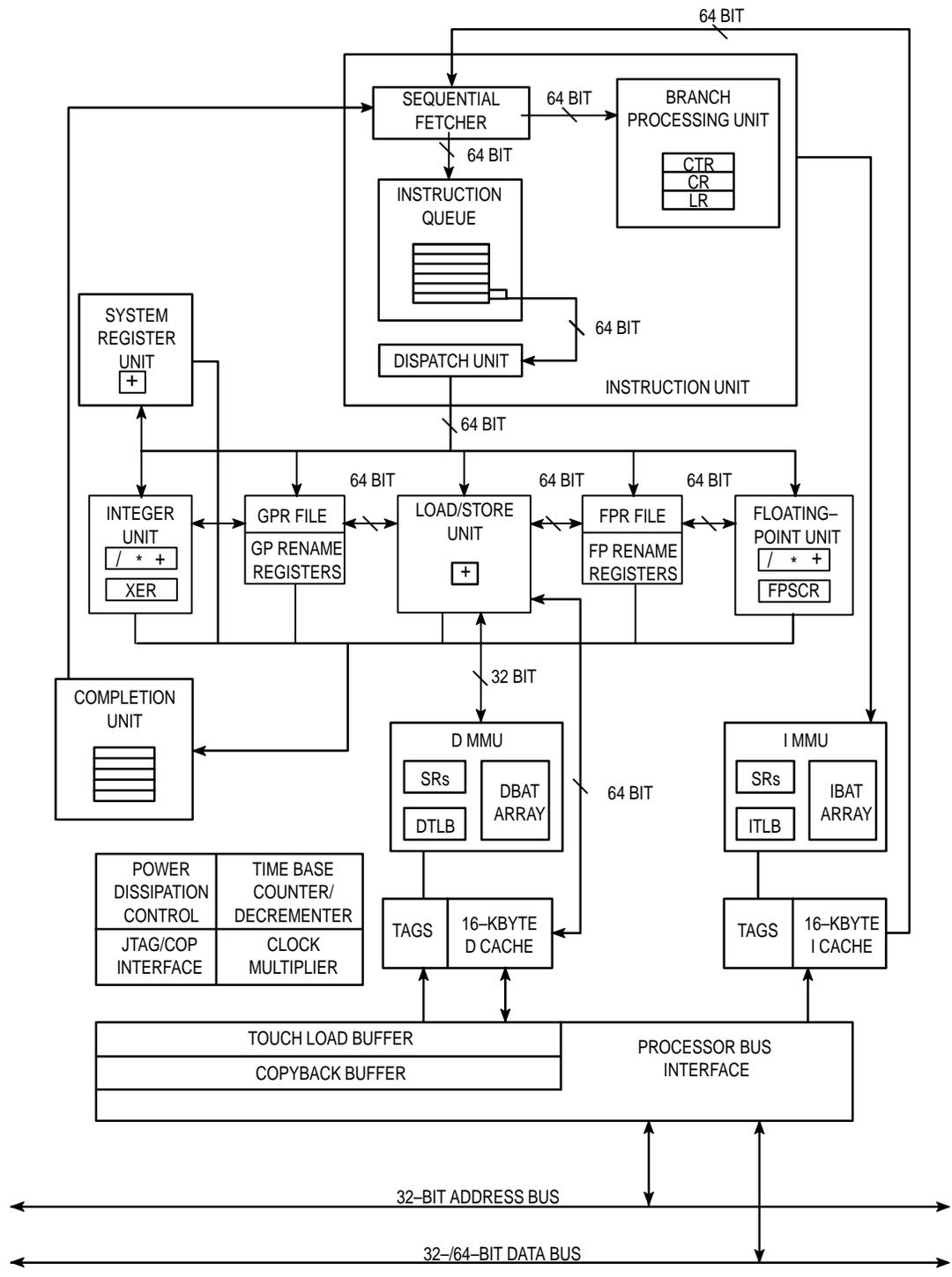


Figure 4. MPC603e Block Diagram

MPC604 RISC Microprocessor

The MPC604 is an implementation of the PowerPC family of RISC microprocessors. The MPC604 implements the PowerPC architecture as it is specified for 32-bit addressing, which provides 32-bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits (single-precision and double-precision). For 64-bit PowerPC implementations, the PowerPC architecture provides additional 64-bit integer data types, 64-bit addressing, and related features.

The MPC604 is a superscalar processor capable of issuing four instructions simultaneously. As many as six instructions can finish execution in parallel. The MPC604 has six execution units that can operate in parallel—floating-point unit (FPU), branch processing unit (BPU), load/store unit (LSU), two single-cycle integer units (SCIUs), and one multiple-cycle integer unit (MCIU).

This parallel design, combined with the PowerPC architecture's specification of uniform instructions that allows for rapid execution times, yields high efficiency and throughput. The MPC604's rename buffers, reservation stations, dynamic branch prediction, and completion unit increase instruction throughput, guarantee in-order completion, and ensure a precise exception model. (Note that the PowerPC architecture specification refers to all exceptions as interrupts.)

The MPC604 has separate memory management units (MMUs) and separate 16-Kbyte on-chip caches for instructions and data. The MPC604 implements two 128-entry, two-way set (64-entry per set) associative translation lookaside buffers (TLBs), one for instructions and one for data, and provides support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and the cache use least-recently used (LRU) replacement algorithms.

The MPC604 has a 64-bit external data bus and a 32-bit address bus. The MPC604 interface protocol allows multiple masters to compete for system resources through a central external arbiter. Additionally, on-chip snooping logic maintains data cache coherency for multiprocessor applications. The MPC604 supports single-beat and burst data transfers for memory accesses and memory-mapped I/O accesses.

The MPC604 uses an advanced, 3.3-V CMOS process technology and is fully compatible with TTL devices.

Block Diagram

Figure 5 provides a block diagram showing features of the MPC604. Note that this is a conceptual block diagram intended to show the basic features rather than an attempt to show how these features are physically implemented on the chip.

MPC604e RISC Microprocessor

The MPC604e is an implementation of the PowerPC family of RISC microprocessors. The MPC604e implements the PowerPC architecture as it is specified for 32-bit addressing, which provides 32-bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits (single-precision and double-precision). For 64-bit PowerPC implementations, the PowerPC architecture provides additional 64-bit integer data types, 64-bit addressing, and related features.

The MPC604e is a superscalar processor capable of issuing four instructions simultaneously. As many as seven instructions can finish execution in parallel. The MPC604e has seven execution units that can operate in parallel—floating-point unit (FPU), branch processing unit (BPU), condition register unit (CRU), load/store unit (LSU), two single-cycle integer units (SCIUs), and one multiple-cycle integer unit (MCIU).

This parallel design, combined with the PowerPC architecture's specification of uniform instructions that allows for rapid execution times, yields high efficiency and throughput. The MPC604e's rename buffers, reservation stations, dynamic branch prediction, and completion unit increase instruction throughput, guarantee in-order completion, and ensure a precise exception model. (Note that the PowerPC architecture specification refers to all exceptions as interrupts.)

The MPC604e has separate memory management units (MMUs) and separate 32-Kbyte on-chip caches for instructions and data. The MPC604e implements two 128-entry, two-way set associative translation lookaside buffers (TLBs), one for instructions and one for data, and provides support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and the cache use least-recently used (LRU) replacement algorithms.

The MPC604e has a 64-bit external data bus and a 32-bit address bus. The MPC604e interface protocol allows multiple masters to compete for system resources through a central external arbiter. Additionally, on-chip snooping logic maintains data cache coherency for multiprocessor applications. The MPC604e supports single-beat and burst data transfers for memory accesses and memory-mapped I/O accesses.

The MPC604e uses an advanced, 2.5-V CMOS process technology and is fully compatible with TTL devices.

Block diagram

Figure 6 provides a block diagram of the MPC604e.

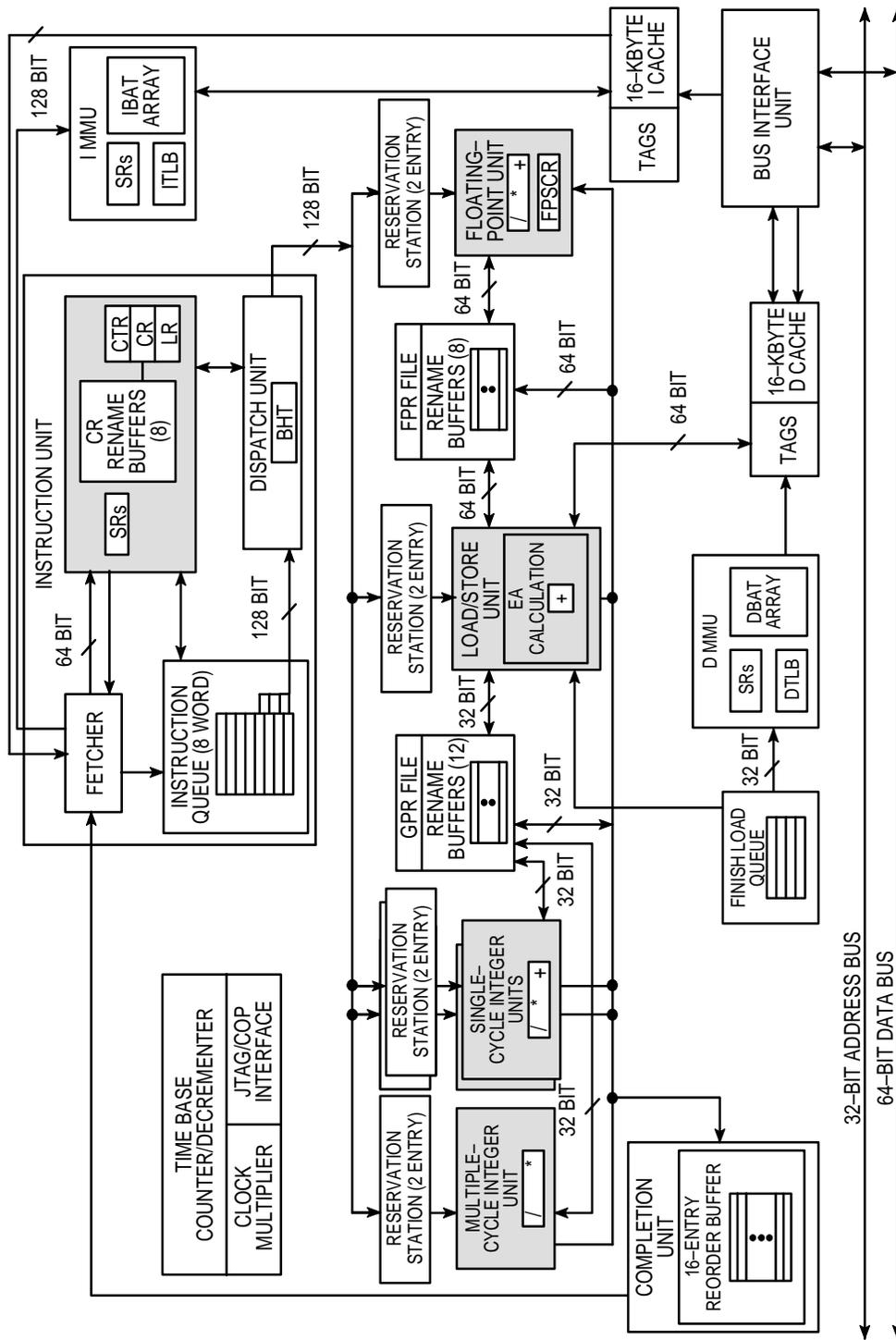


Figure 5. MPC604 Block Diagram

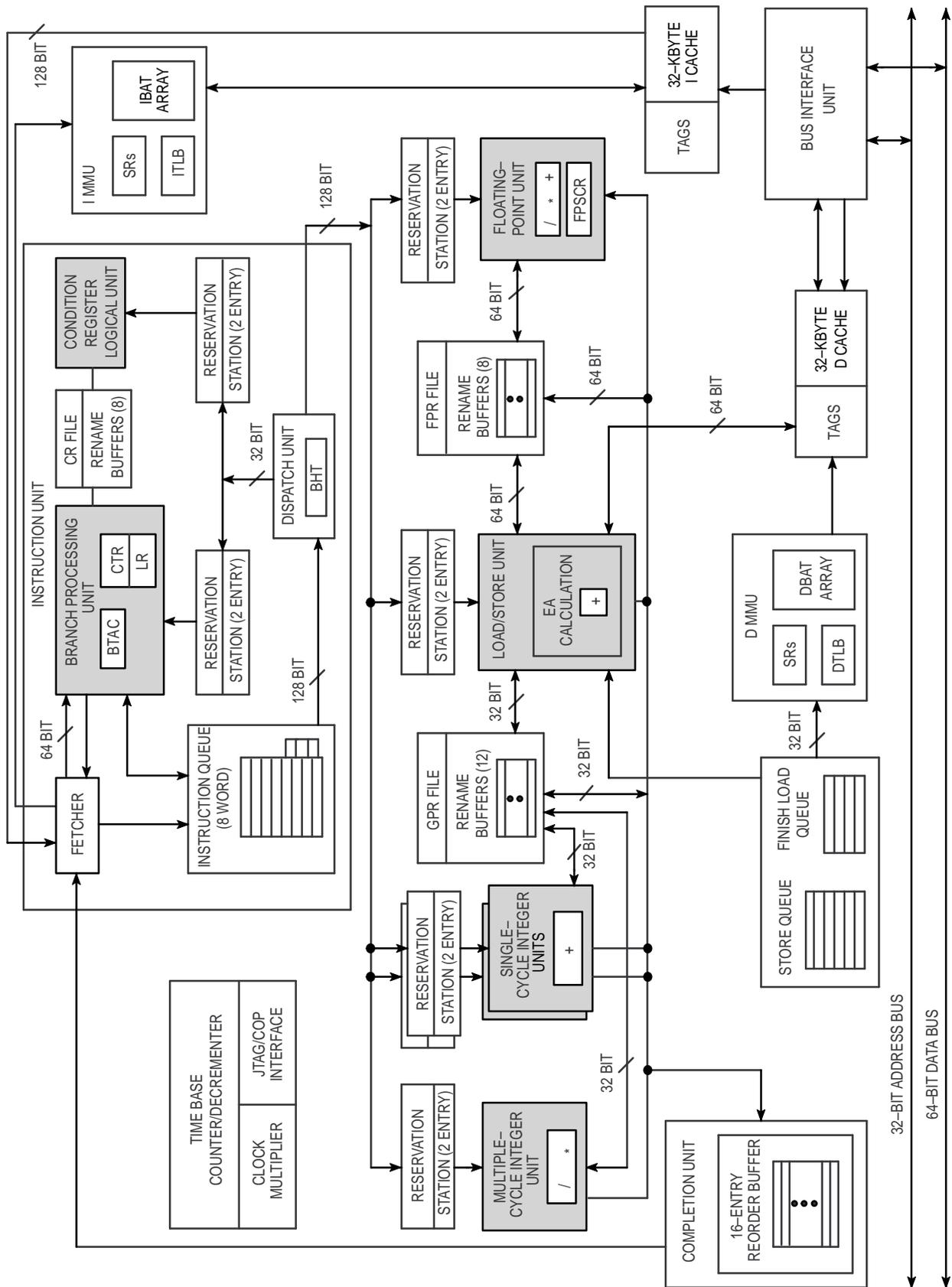


Figure 6. MPC604e Block Diagram

New Features of the MPC604e

Features of the MPC604e that are not implemented in the MPC604 are as follows:

- Additional special-purpose registers
 - HID1 provides four read-only PLL_CFG bits for indicating the processor/bus clock ratio.
 - Three additional registers support the performance monitor—MMCR1 is a second control register that includes bits to support the use of two additional counter registers, PMC3 and PMC4.
- Instruction execution
 - Separate units for branch and condition register (CR) instructions. The BPU is now split into a CR logical unit and a branch unit, which makes it possible for branch instructions to execute and resolve before preceding CR logical instructions. The MPC604e can still only dispatch one CR logical or branch instruction per cycle, but it can execute both branch and CR logical instructions at the same time.
 - Branch correction in decode stage. Branch correction in the decode stage can now predict branches whose target is taken from the count or link registers if no updates of the count and link register are pending. This saves at least one cycle on branch correction when the **mtspr** instruction can be sufficiently separated from the branch that uses the SPR as a target address.
 - Ability to disable the branch target address cache (BTAC)—HID0[30] has been defined to allow the BTAC to be disabled. When HID0[30] is set, the BTAC contents are invalidated and the BTAC behaves as if it were empty. New entries cannot be added until the BTAC is enabled.
- Improvements to cache implementation
 - 32-Kbyte split data and instruction caches. Like the 604, both caches are four-way set associative; however, each cache has twice as many sets, logically separated into 128 sets of odd lines and 128 sets of even lines.
 - Data cache line-fill buffer forwarding. In the 604 only the critical double word of a burst operation was made available to the requesting unit at the time it was burst into the line-fill buffer. Subsequent data was unavailable until the cache block was filled. On the MPC604e, subsequent data is also made available as it arrives in the line-fill buffer.
 - Additional cache copyback buffers. The MPC604e implements three copyback write buffers (as opposed to one in the 604). Having multiple copyback buffers provides the ability for certain instructions to take fuller advantage of the pipelined system bus to provide more efficient handling of cache copyback, block invalidate operations caused by the data cache block flush (**dcbf**) instruction, and cache block clean operations resulting from the data cache block store (**dcbst**) instruction.
- Coherency support for instruction fetching. Instruction fetching coherency is controlled by HID0[23]. In the default mode, HID0[23] is 0, GBL is not asserted for instruction accesses, as is the case with the 604. If the bit is set, and instruction translation is enabled (MSR[IR] = 1), the GBL signal is set to reflect the M bit for this page or block. If instruction translation is disabled (MSR[IR] = 0), the GBL signal is asserted.
- System interface operation
 - The MPC604e has the same pin configuration as the MPC604; however, on the MPC604e V_{DD} and AV_{DD} must be connected to 2.5 Vdc and OV_{DD} must be connected to 3.3 Vdc. The MPC604e uses split voltage planes, and for replacement compatibility, MPC604/MPC604e designs should provide both 2.5-V and 3.3-V planes and the ability to connect those two planes together and disable the 2.5-V plane for operation with an MPC604.
 - Support for additional processor/bus clock ratios (5:2 and 4:1). Configuration of the processor/bus clock ratios is displayed through a new MPC604e-specific register, HID1.
 - To support the changes in the clocking configuration, different precharge timings for the ABB, DBB, ARTRY, and SHD signals are implemented internally by the processor. The precharge timings for ARTRY and SHD can be disabled by setting HID0[7].
 - No-DRTRY mode. In addition to the normal and fast L2 modes implemented on the 604, a no-DRTRY mode is implemented on the MPC604e that improves performance on read operations for systems that do not use the DRTRY signal. No-DRTRY mode makes read data available to the processor one bus clock cycle sooner than in normal mode. In no-DRTRY mode, the DRTRY signal is no longer sampled as part of a qualified bus grant.
- Full hardware support for little-endian accesses. Little-endian accesses take alignment exceptions for only the same set of causes as big-endian accesses. Accesses that cross a word boundary require two accesses with the lower-addressed word accessed first.
- Additional enhancements to the performance monitor.

MPC620 RISC Microprocessor

The MPC620 is an implementation of the PowerPC™ family of RISC microprocessors. The MPC620 implements the PowerPC architecture as it is specified for 64-bit addressing, which provides 64-bit effective (logical) addresses, integer data types of 8, 16, 32, and 64 bits, and floating-point data types of 32 and 64 bits (single-precision and double-precision). The MPC620 is software compatible with the 32-bit versions of the PowerPC microprocessor family.

The MPC620 is a superscalar processor capable of issuing four instructions simultaneously. As many as six instructions can finish execution in parallel. The MPC620 has six execution units that can operate in parallel — floating-point unit (FPU), branch processing unit (BPU), load/store unit (LSU), two single-cycle integer units (SCIUs), and one multiple-cycle integer unit (MCIU).

This parallel design, combined with the PowerPC architecture's specification of uniform instructions that allows for rapid execution times, yields high efficiency and throughput. The MPC620's rename buffers, reservation stations, dynamic branch prediction, and completion unit increase instruction throughput, guarantee in-order completion, and ensure a precise exception model.

The MPC620 has separate memory management units (MMUs) and separate 32-Kbyte on-chip caches for instructions and data. The MPC620 implements a 128-entry, two-way set-associative translation lookaside buffer (TLB) for instructions and data, and provides support for demand-paged virtual memory address translation and variable-sized block translation. The TLB and the cache use least-recently used (LRU) replacement algorithms.

The MPC620 has a 40-bit address bus, and can be configured with either a 64- or 128-bit data bus. The MPC620 interface protocol allows multiple masters to compete for system resources through a central external arbiter. Additionally, on-chip snooping logic maintains data cache coherency for multiprocessor applications. The MPC620 supports single-beat and burst data transfers for memory accesses and memory-mapped I/O accesses.

The MPC620 uses an advanced, 3.3-V CMOS process technology and is compatible with 3.3-V CMOS devices.

Block Diagram

Figure 7 provides a block diagram showing features of the MPC620. Note that this is a conceptual block diagram intended to show the basic features rather than an attempt to show how these features are physically implemented on the chip.

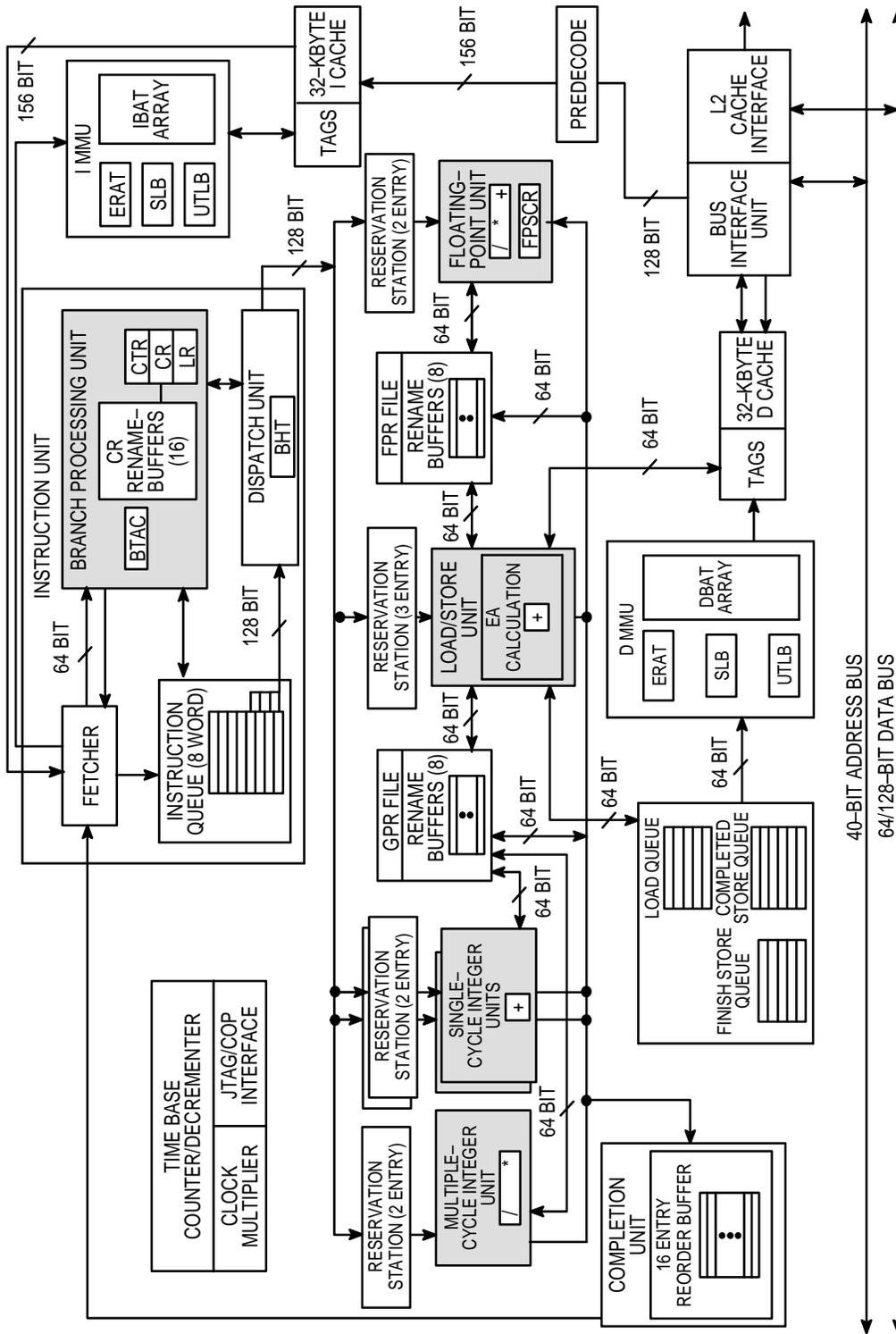


Figure 7. MPC620 Block Diagram

MPC105 PCI Bridge/Memory Controller

The MPC105 PCI bridge/memory controller (PCIB/MC) provides a PowerPC reference platform-compliant bridge between the PowerPC microprocessor family and the peripheral component interconnect (PCI) bus. PCI support allows system designers to rapidly design systems using peripherals already designed for PCI and the other standard interfaces available in the personal computer hardware environment. The MPC105 integrates secondary cache control and a high-performance memory controller that supports DRAM, SDRAM, ROM, and Flash ROM. The MPC105 uses an advanced, 3.3-V CMOS process technology and is fully compatible with TTL devices.

The MPC105 provides an integrated high bandwidth, high performance, TTL-compatible interface between a 60x processor, a secondary (L2) cache or secondary 60x processor, the PCI bus, and main memory.

The MPC105 supports a programmable interface to a variety of PowerPC microprocessors operating at various bus speeds. The 60x processor interface uses a subset of the 60x bus protocol, which enables the interface between the processor and MPC105 to be optimized for performance. The MPC105's 60x interface allows for a variety of system configurations by providing support for either a direct-mapped, lookaside, L2 cache or a secondary 60x processor. The L2 cache interface generates the arbitration and support signals necessary to maintain a write-through or

write-back L2 cache. The L2 cache interface supports either burst SRAMs or asynchronous SRAMs, and L2 data a per-byte basis. The MPC105 features on-chip byte decoding for L2 data write enables or can be configured to use external logic for data write enable generation.

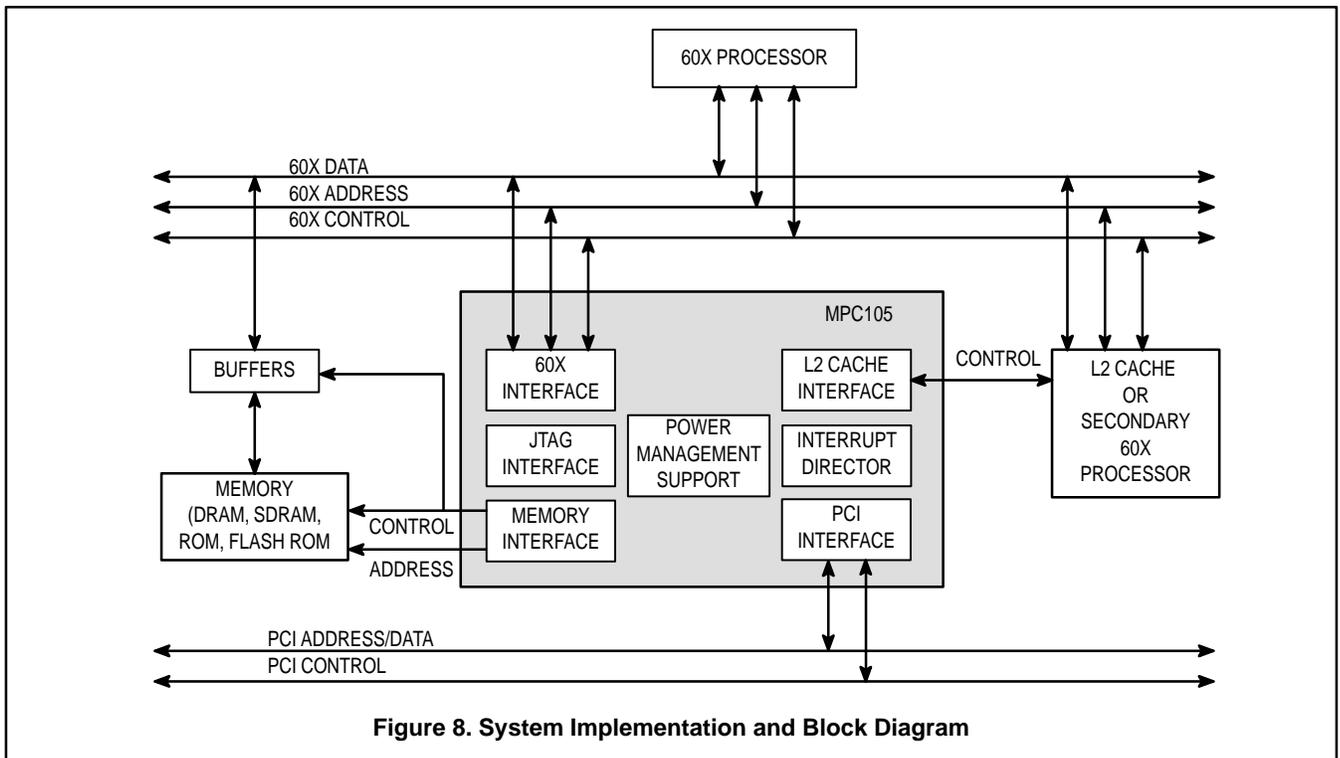
The PCI interface connects the processor and memory buses to the PCI bus, to which I/O components are connected, without the need for "glue" logic. This interface acts as both a master and slave device.

The memory interface controls processor and PCI interactions to main memory. It is capable of supporting a variety of DRAM or SDRAM, and ROM or Flash ROM configurations as main memory. The maximum supported memory size is 1 Gbyte of DRAM or SDRAM, with 16 Mbytes of ROM or 1 Mbyte of Flash ROM.

The MPC105 provides hardware support for four levels of power reduction; the doze, nap, and sleep modes are invoked by register programming, and the suspend mode is invoked by assertion of an external signal. The design of the MPC105 is fully static, allowing internal logic states to be preserved during all power saving modes. The following sections describe the programmable power modes provided by the MPC105.

Block Diagram

Figure 8 shows the MPC105 in a typical system implementation. The major functional units within the MPC105 are also shown in Figure 1. Note that this is a conceptual block diagram intended to show the basic features rather than an attempt to show how these features are physically implemented on the device.



MPC106 PCI Bridge/Memory Controller

The MPC106 provides a PowerPC common hardware reference platform (CHRP) compliant bridge between the PowerPC microprocessor family and the Peripheral Component Interconnect (PCI) bus. PCI support allows system designers to rapidly design systems using peripherals already designed for PCI and the other standard interfaces available in the personal computer hardware environment. The MPC106 integrates secondary cache control and a high-performance memory controller. The MPC106 uses an advanced, 3.3-V CMOS process technology and is fully compatible with TTL devices.

The MPC106 provides an integrated high-bandwidth, high-performance, TTL-compatible interface between a 60x processor, a secondary (L2) cache or secondary 60x processor, the PCI bus, and main memory.

60x Processor Interface

The MPC106 supports a programmable interface to a variety of PowerPC microprocessors operating at select bus speeds. The 60x processor interface of the MPC106 uses a subset of the 60x bus protocol, supporting single-beat and burst data transfers. The address bus is 32 bits wide and the data bus is 64 bits wide. The address and data buses are decoupled to support pipelined transactions. PCI bus accesses to system memory space are passed to the 60x processor bus for snooping purposes. Two signals on the MPC106, LBCLAIM, and DBGLB, are provided for an optional local bus slave. The local bus slave must be capable of generating AACK and TA signals to interact with the 60x processor(s). Depending on the system implementation, the processor(s) may operate at the PCI bus clock rate, or at two or three times the PCI bus clock rate. The bus is synchronous, with all timing relative to the rising edge of the bus clock.

L2 Cache/Multiple Processor Interface

The MPC106 provides support for the following configurations of 60x processors and L2 cache:

- A single 60x processor with no L2 cache
- A single 60x processor plus a direct-mapped, lookaside, L2 cache
- A single 60x processor plus an external L2 cache controller or integrated L2 cache module such as the Motorola MPC2604GA integrated L2 lookaside cache
- Two 60x processors with no L2 cache
- Two 60x processors plus an external L2 cache controller or integrated L2 cache module such as the Motorola MPC2604GA integrated L2 lookaside cache

The internal L2 cache controller generates the arbitration and support signals necessary to maintain a write-through or write-back L2 cache. The internal L2 cache controller supports either asynchronous SRAMs, pipelined burst SRAMs, or synchronous burst SRAMs, using byte parity for data error detection. When a second 60x processor is used, three signals of the L2 interface (BR1, BG1, and DBG1) change their functions to allow for arbitration between the 60x processors. All 60x interface signals of the MPC106, except the bus request, bus grant, and data bus grant signals, are shared by the 60x processors. When an external L2 controller (or integrated L2 cache module) is used, three signals of the L2 interface (BRL2, BGL2, and DBGL2) change their functions to allow the MPC106 to arbitrate between the external cache and the 60x processor(s).

Memory Interface

The memory interface controls processor and PCI interactions to main memory and is capable of supporting a variety of DRAM, or extended data-out (EDO) DRAM and ROM or Flash ROM configurations as main memory. The maximum supported memory size is 1 Gbyte of DRAM or EDO DRAM, with 16 Mbytes of ROM or Flash ROM. The memory controller of the MPC106 supports the various memory sizes through software initialization of on-chip configuration registers. Parity or ECC is provided for error detection.

PCI Interface

The MPC106's PCI interface is compliant with the PCI *Local Bus Specification, Revision 2.1*, and follows the guidelines in the *PCI System Design Guide, Revision 1.0* for host bridge architecture. The PCI interface connects the processor and memory buses to the PCI bus, to which I/O components are connected. The PCI bus uses a 32-bit multiplexed address/data bus, plus various control and error signals.

Figure 9 shows the major functional units within the MPC106. Note that this is a conceptual block diagram intended to show the basic features rather than an attempt to show how these features are physically implemented on the device.

