TL082 Wide Bandwidth Dual JFET Input Operational Amplifier

General Description
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

Features
- Internally trimmed offset voltage 15 mV
- Low input bias current 50 pA
- Low input noise voltage 16 nV/√Hz
- Low input noise current 0.01 pA/√Hz
- Wide gain bandwidth 4 MHz
- High slew rate 13 V/µs
- Low supply current 3.6 mA
- High input impedance 10^12 Ω
- Low total harmonic distortion AV = 10, <0.02%
- Rf = 10k, VO = 20 Vp – p.
- BW = 20 Hz–20 kHz
- Low 1/f noise corner 50 Hz
- Fast settling time to 0.01% 2 µs

Typical Connection

Connection Diagram
Order Number TL082CM or TL082CP
See NS Package Number M08A or N08E

Simplified Schematic

BI-FET II™ is a trademark of National Semiconductor Corp.
Absolute Maximum Ratings
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage: ±18V
Power Dissipation (Note 1): 250°C
Operating Temperature Range: 0°C to +70°C

DC Electrical Characteristics (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>TL082C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
</tr>
<tr>
<td>VOS</td>
<td>Input Offset Voltage</td>
<td>RS = 10 kΩ, TA = 25°C</td>
<td>5</td>
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<tr>
<td></td>
<td></td>
<td>Over Temperature</td>
<td>mV</td>
</tr>
<tr>
<td>ΔVOS/ΔT</td>
<td>Average TC of Input Offset Voltage</td>
<td>RS = 10 kΩ</td>
<td>10</td>
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<tr>
<td>IOS</td>
<td>Input Offset Current</td>
<td>TJ = 25°C, (Notes 4, 5)</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TJ ≤ 70°C</td>
<td>pA</td>
</tr>
<tr>
<td>IB</td>
<td>Input Bias Current</td>
<td>TJ = 25°C, (Notes 4, 5)</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TJ ≤ 70°C</td>
<td>pA</td>
</tr>
<tr>
<td>Rin</td>
<td>Input Resistance</td>
<td>TJ = 25°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10^12</td>
</tr>
<tr>
<td>AVOL</td>
<td>Large Signal Voltage Gain</td>
<td>VS = ±15V, TA = 25°C</td>
<td>25</td>
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<tr>
<td></td>
<td></td>
<td>VS = ±10V, RL = 2 kΩ</td>
<td>15</td>
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<td></td>
<td></td>
<td>Over Temperature</td>
<td></td>
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<tr>
<td>VO</td>
<td>Output Voltage Swing</td>
<td>VS = ±15V, RL = 10 kΩ</td>
<td>±12</td>
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<td></td>
<td></td>
<td>Over Temperature</td>
<td>15</td>
</tr>
<tr>
<td>VCM</td>
<td>Input Common-Mode Voltage Range</td>
<td>VS = ±15V</td>
<td>±11</td>
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<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td>RS ≤ 10 kΩ</td>
<td>70</td>
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<tr>
<td>PSRR</td>
<td>Supply Voltage Rejection Ratio</td>
<td>(Note 6)</td>
<td>70</td>
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<tr>
<td>I0</td>
<td>Supply Current</td>
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<td>3.6</td>
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</table>

AC Electrical Characteristics (Note 4)

<table>
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<tr>
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<th>Parameter</th>
<th>Conditions</th>
<th>TL082C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
</tr>
<tr>
<td></td>
<td>Amplifier to Amplifier Coupling</td>
<td>TA = 25°C, f = 1Hz-20 kHz (Input Referred)</td>
<td>−120</td>
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<td>SR</td>
<td>Slew Rate</td>
<td>VS = ±15V, TA = 25°C</td>
<td>8</td>
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<td>GBW</td>
<td>Gain Bandwidth Product</td>
<td>VS = ±15V, TA = 25°C</td>
<td>4</td>
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<tr>
<td>eN</td>
<td>Equivalent Input Noise Voltage</td>
<td>TA = 25°C, RS = 100Ω, f = 1000 Hz</td>
<td>25</td>
</tr>
<tr>
<td>IE</td>
<td>Equivalent Input Noise Current</td>
<td>TJ = 25°C, f = 1000 Hz</td>
<td>0.01</td>
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</tbody>
</table>

**Note 1:** For operating at elevated temperatures, the device must be derated based on a thermal resistance of 115°C/W junction to ambient for the N package.

**Note 2:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 3:** The power dissipation limit, however, cannot be exceeded.

**Note 4:** These specifications apply for VS = ±15V and 0°C ≤ TA ≤ +70°C. VOS, IB and IOS are measured at VCM = 0.

**Note 5:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, TJ. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, PD. TJ = TA + θJA·PD where θJA is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

**Note 6:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. VS = ±6V to ±15V.
Typical Performance Characteristics (Continued)

- Distortion vs Frequency
- Undistorted Output Voltage Swing
- Open Loop Frequency Response

- Common-Mode Rejection Ratio
- Power Supply Rejection Ratio
- Equivalent Input Noise Voltage

- Open Loop Voltage Gain (V/V)
- Output Impedance
- Inverter Settling Time
Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (Bi-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case
Application Hints (Continued)
does a latch occur since raising the input back within
the common-mode range again puts the input stage and thus
the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input
will not change the phase of the output; however, if both
inputs exceed the limit, the output of the amplifier will be
forced to a high state.

The amplifiers will operate with a common-mode input volt-
age equal to the positive supply; however, the gain band-
width and slew rate may be decreased in this condition.

When the negative common-mode voltage swings to within
3V of the negative supply, an increase in input offset voltage
may occur.

Each amplifier is individually biased by a zener reference
which allows normal circuit operation on ±6V power sup-
plies. Supply voltages less than these may result in lower
gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V
over the full temperature range of 0°C to +70°C. If the am-
plifier is forced to drive heavier load currents, however, an
increase in input offset voltage may occur on the negative
voltage swing and finally reach an active current limit on
both positive and negative swings.

Precautions should be taken to ensure that the power sup-
ply for the integrated circuit never becomes reversed in po-
larly or that the unit is not inadvertently installed backwards
in a socket as an unlimited current surge through the result-
ing forward diode within the IC could cause fusing of the
internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET
input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead
dress, component placement and supply decoupling in or-
der to ensure stability. For example, resistors from the out-
put to an input should be placed with the body close to the
input to minimize “pick-up” and maximize the frequency of
the feedback pole by minimizing the capacitance from the
input to ground.

A feedback pole is created when the feedback around any
amplifier is resistive. The parallel resistance and capaci-
tance from the input of the device (usually the inverting in-
put) to AC ground set the frequency of the pole. In many
instances the frequency of this pole is much greater than
the expected 3 dB frequency of the closed loop gain and
consequently there is negligible effect on stability margin.

However, if the feedback pole is less than approximately 6
times the expected 3 dB frequency a lead capacitor should
be placed from the output to the input of the op amp. The
value of the added capacitor should be such that the RC
time constant of this capacitor and the resistance it parallels
is greater than or equal to the original feedback pole time
constant.

Detailed Schematic

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TL/H/8357-11
Typical Applications

Three-Band Active Tone Control

1. All controls flat.
2. Bass and treble boost, mid flat.
4. Mid boost, bass and treble flat.
5. Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications
Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier

\[ A_V = \left( \frac{2R_2}{R_1} + 1 \right) \frac{R_5}{R_4} \]

\( \oplus \) and \( \ominus \) are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With \( A_V = 1400 \), resistor matching \( 0.01\% \): CMRR = 136 dB

- Very high input impedance
- Super high CMRR

Fourth Order Low Pass Butterworth Filter

- Corner frequency \( f_c \) = \( \sqrt{\frac{R_1 R_2 CC_1}{2\pi}} \)
- Passband gain \( H_0 \) = \( \frac{1}{1 + \frac{R_4'}{R_3'}} \frac{1}{1 + \frac{R_4}{R_3}} \)
- First stage \( Q \) = 1.31
- Second stage \( Q \) = 0.541

- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance
Typical Applications (Continued)

Fourth Order High Pass Butterworth Filter

- Corner frequency \( f_c \) = \( \frac{1}{\sqrt{R_1 R_2 C_2}} \) [eq]
- Passband gain \( H_0 \) = \( (1 + \frac{R_4}{R_3})(1 + \frac{R_4'}{R_3'}) \) [eq]
- First stage \( Q = 1.31 \)
- Second stage \( Q = 0.541 \)
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

Ohms to Volts Converter

\[ V_O = \frac{5V}{R_{LADDER}} \times R_X \]

Where \( R_{LADDER} \) is the resistance from switch S1 pole to pin 7 of the TL082CP.
Physical Dimensions inches (millimeters)

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