MACH® 4 Family

High Performance EE CMOS Programmable Logic With Maximum Ease Of Use

DISTINCTIVE CHARACTERISTICS

- **High-performance, EE CMOS CPLD family**
- **SpeedLocking™ for guaranteed fixed timing (-7/10/12/15 ns t_{PD})**
- **High density**
  - 1250-10,000 PLD Gates
  - 44-208 Pins
  - 32-384 Registers
- **32-256 macrocells**
  - D/T,J-K,S-R Registers and latches
  - Synchronous or asynchronous mode
  - Programmable polarity
  - Reset/preset swapping
- **Central, input, and output switch matrices**
  - 100% Routability
- **Input and output switch matrices for 100% pin-out retention**
- **JTAG in-system programmable**
- **Up to 20 product terms per macrocell, with XOR**
- **Registered/latched inputs**
- **Synchronous and asynchronous modes for each macrocell**
  - Clock generator in each PAL® block for programmable clocks, edges in either mode
  - Individual clock, initialization product terms in asynchronous mode
- **Extensive software development support**
- **Third-party hardware programming support**

PRODUCT SELECTOR GUIDE

Device	Package	Macrocells	I/Os	Dedicated Inputs	Output Enables	Flip-Flops	Commercial		Industrial	t_{SS} (ns)	t_{CO} (ns)	I_{CC} Static (mA)
							t_{PD} (ns)	f_{CNT} (MHz)	t_{PD} (ns)			
M4(LV)-32	44 PLCC 44 TQFP	32	32	2	32	32	7.5	133	10	5.5	5.5	35
M4(LV)-64	44 PLCC 44 TQFP	64	32	2	32	96	7.5	133	10	5.5	5.5	55
M4(LV)-96	100 TQFP	96	48	8	48	144	7.5	133	10	5.5	5.5	60
M4-96	144 PQFP	96	96	6	96	96	15	66.6	NA	NA	NA	188
M4(LV)-128	100 PQFP 100 TQFP	128	64	6	64	192	7.5	133	10	5.5	5.5	70
M4(LV)-128N	84 PLCC	128	64	6	64	192	7.5	133	10	5.5	5.5	70
M4(LV)-192	144 TQFP	192	96	16	96	288	10	100	12	6	6.5	85
M4(LV)-256	208 PQFP	256	128	14	128	384	10	100	12	6	6.5	100

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Amendment/**0** Issue Date: **August 1997**

GENERAL DESCRIPTION

The MACH® 4 family from Vantis offers an exceptionally flexible architecture and delivers a superior CPLD solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost in design and manufacturing. The MACH 4 CPLDs are members of Vantis' high-performance 0.35-micron process and offer densities ranging from 32 to 256 macrocells with 100% utilization and 100% pin-out retention.

All MACH 4 family members deliver first-time fit and easy system integration with pin-out retention after any design change and refit.With multi-tiered central switch matrices, enhanced logic arrays, intelligent logic allocator with an XOR gate and multi-clocking, the MACH 4 family has synchronous/asynchronous logic and flexible set/reset capabilities. For both 3.3-V and 5-V operations, the MACH 4 products can deliver guaranteed fixed timing as fast as 7.5 ns t_{PD} and 133 MHz f_{CNT} through the SpeedLocking feature when using up to 20 product terms per output.

The MACH 4 family offers 6 density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP) and Plastic Leaded Chip Carrier (PLCC) ranging from 44 to 208 pins. It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly™ inputs and I/Os, programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

All MACH 4 products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1149.1) interface. JTAG boundary scan testing capability also allows product testability on automatic test equipment for device connectivity.

Vantis offers software design support for MACH devices through its own development system and device fitters integrated into third-party CAE tools. Platform support extends across PCs, Sun and HP workstations under advanced operating systems such as Windows 3.1, Windows 95 and NT, SunOS and Solaris, and HPUX.

MACHXL® software is a complete development system for the PC, supporting Vantis' MACH devices. It supports design entry with Boolean and behavioral syntax, state machine syntax and truth tables. Functional simulation and static timing analysis are also included in this easy-to-use system. This development system includes high-performance device fitters for all MACH devices.

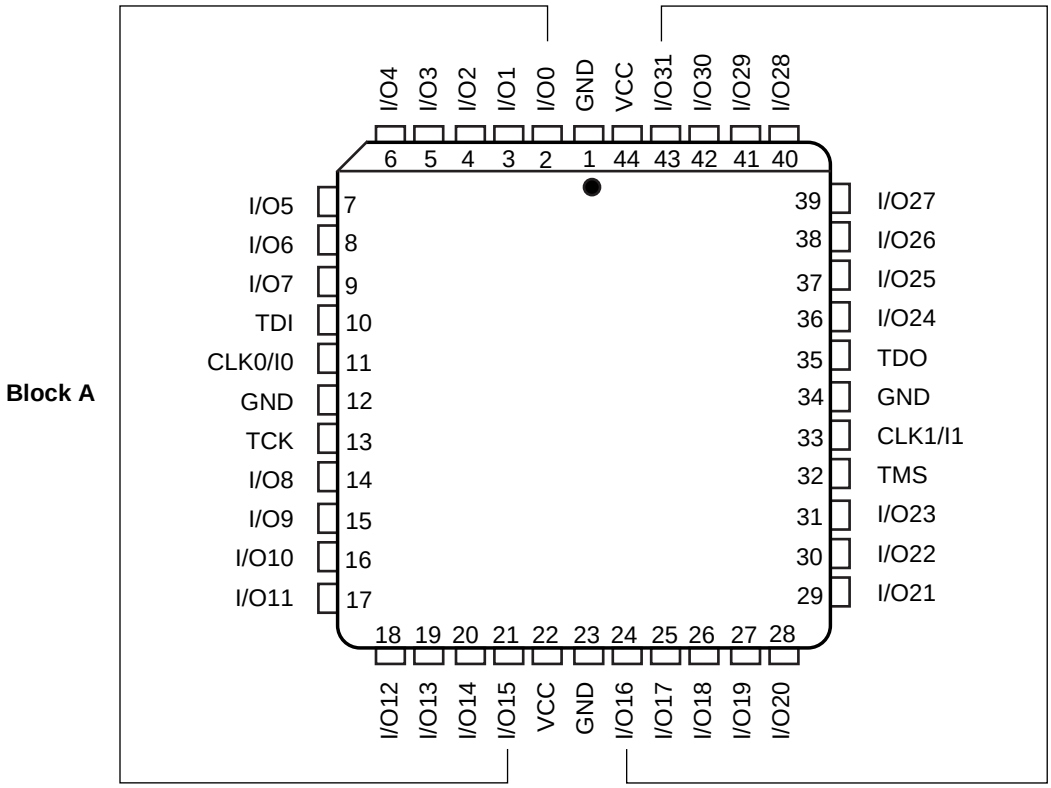
The same fitter technology included in MACHXL software is seamlessly incorporated into third-party tools from leading CAE vendors such as Synario, Viewlogic, Mentor Graphics, Cadence and MINC. Interface kits and MACHXL configurations are also available to support design entry and verification with other leading vendors such as Synopsys, Exemplar, OrCAD, Synplicity and Model Technology. These MACHXL configurations and interfaces accept EDIF 2.0.0 netlists, generate JEDEC files for MACH devices, and create industry-standard SDF, VITAL-compliant VHDL and Verilog output files for design simulation.

Vantis offers in-system programming support for MACH devices through its MACHPRO® software enabling MACH device programmability through JTAG compliant ports and easy-to-use PC interface. Additionally, MACHPRO generated vectors work seamlessly with HP3070, GenRad and Teradyne testers to program MACH devices or test them for connectivity.

CONNECTION DIAGRAM (M4(LV)-32)

Top View

44-Pin PLCC



17466E-1

Note:
Advance information for the M4(LV)-32.

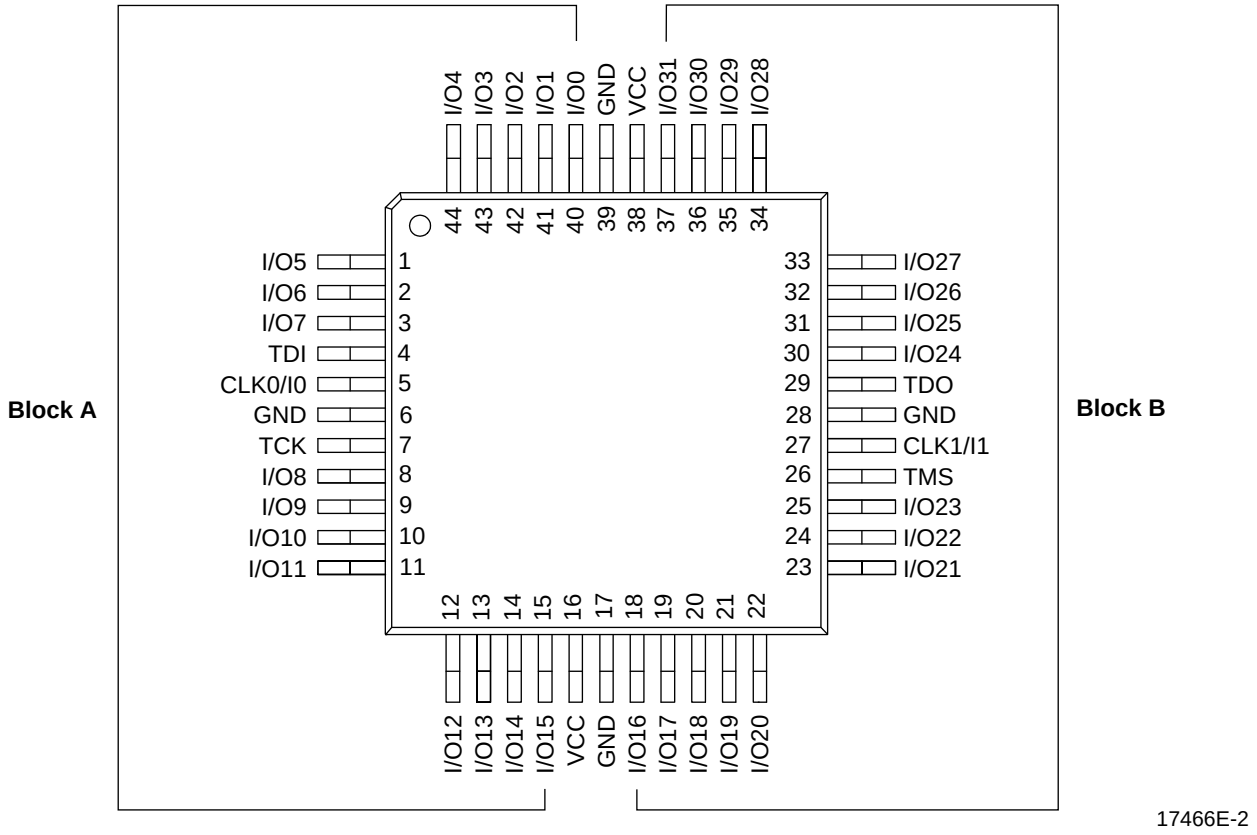
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

CONNECTION DIAGRAM (M4(LV)-32)

Top View

44-Pin TQFP



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Note:
Advance information for the M4(LV)-32.

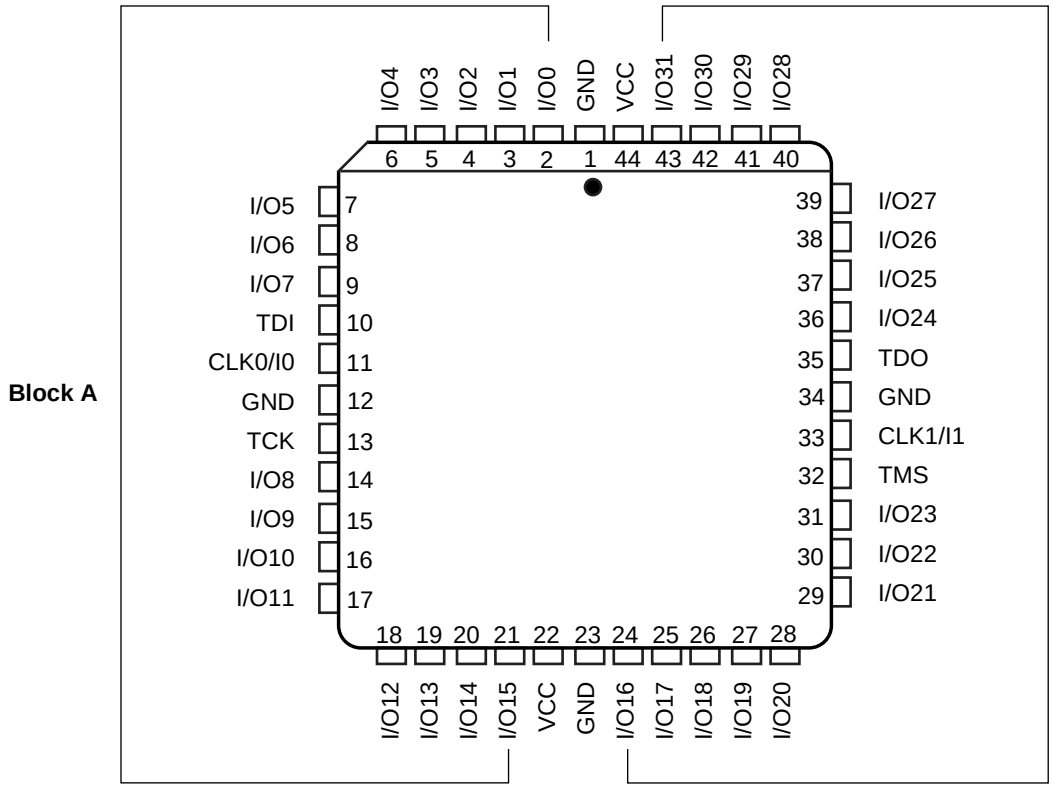
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

CONNECTION DIAGRAM (M4(LV)-64)

Top View

44-Pin PLCC



17466E-3

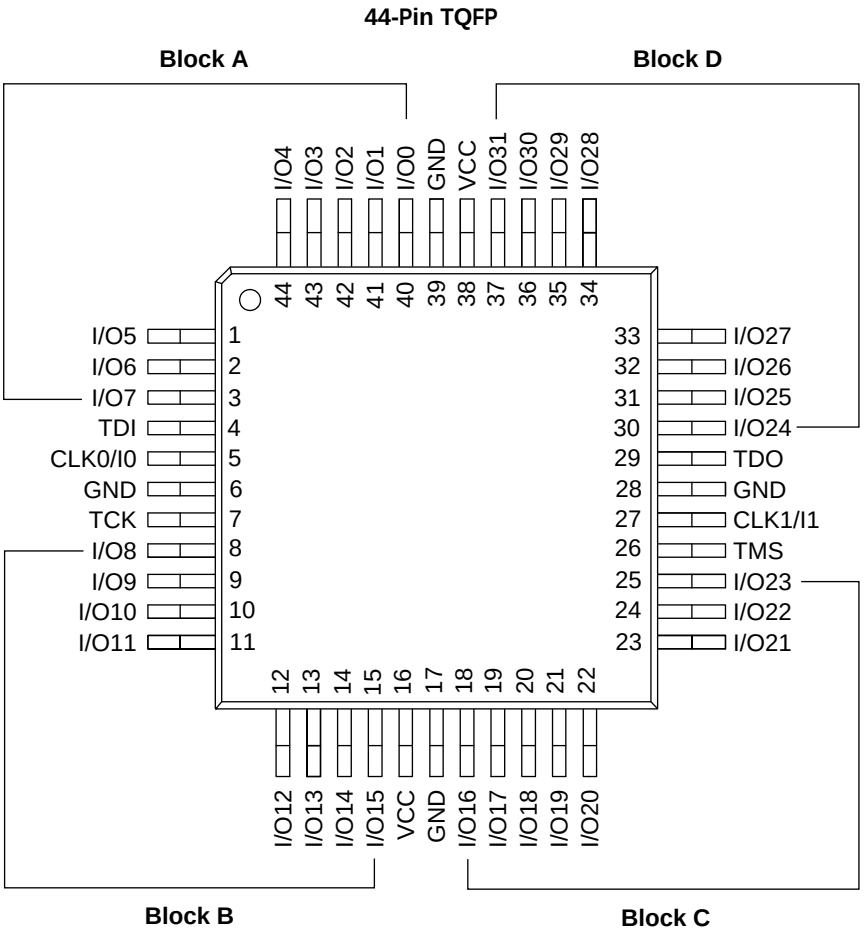
Note:
Advance information for the M4(LV)-64.

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

CONNECTION DIAGRAM (M4(LV)-64)

Top View



17466E-4

Note:
Advance information for the M4(LV)-64.

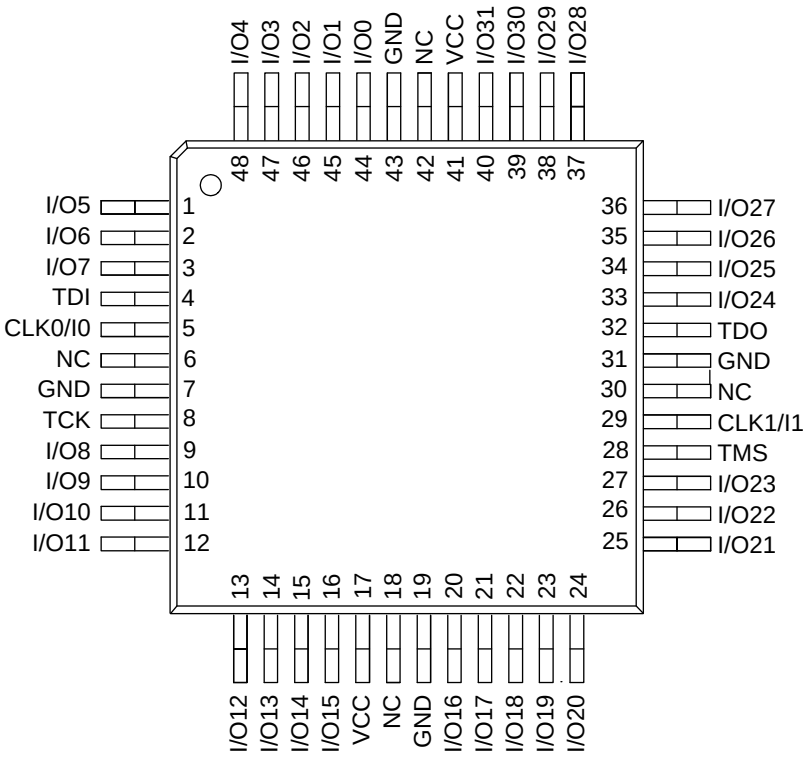
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

CONNECTION DIAGRAM (M4(LV)-32 and M4(LV)-64)

Top View

48-Pin TQFP



17466E-5

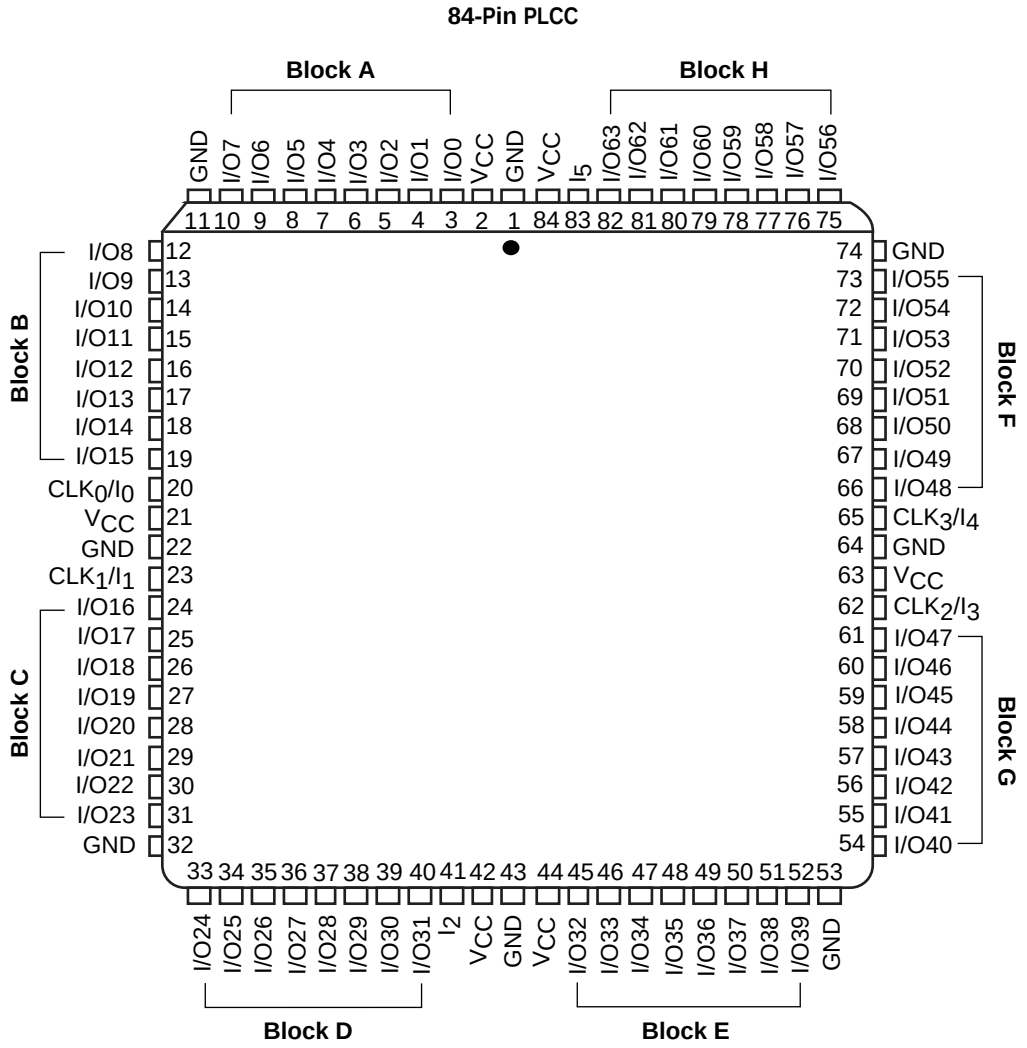
Note:
Advance information. Pin-compatible with the M4(LV)-32 and the M4(LV)-64.

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
NC = No Connect
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

CONNECTION DIAGRAM (M4(LV)-128N)

Top View



Note:
Pin-compatible with the MACH131, MACH231, and MACH435.

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

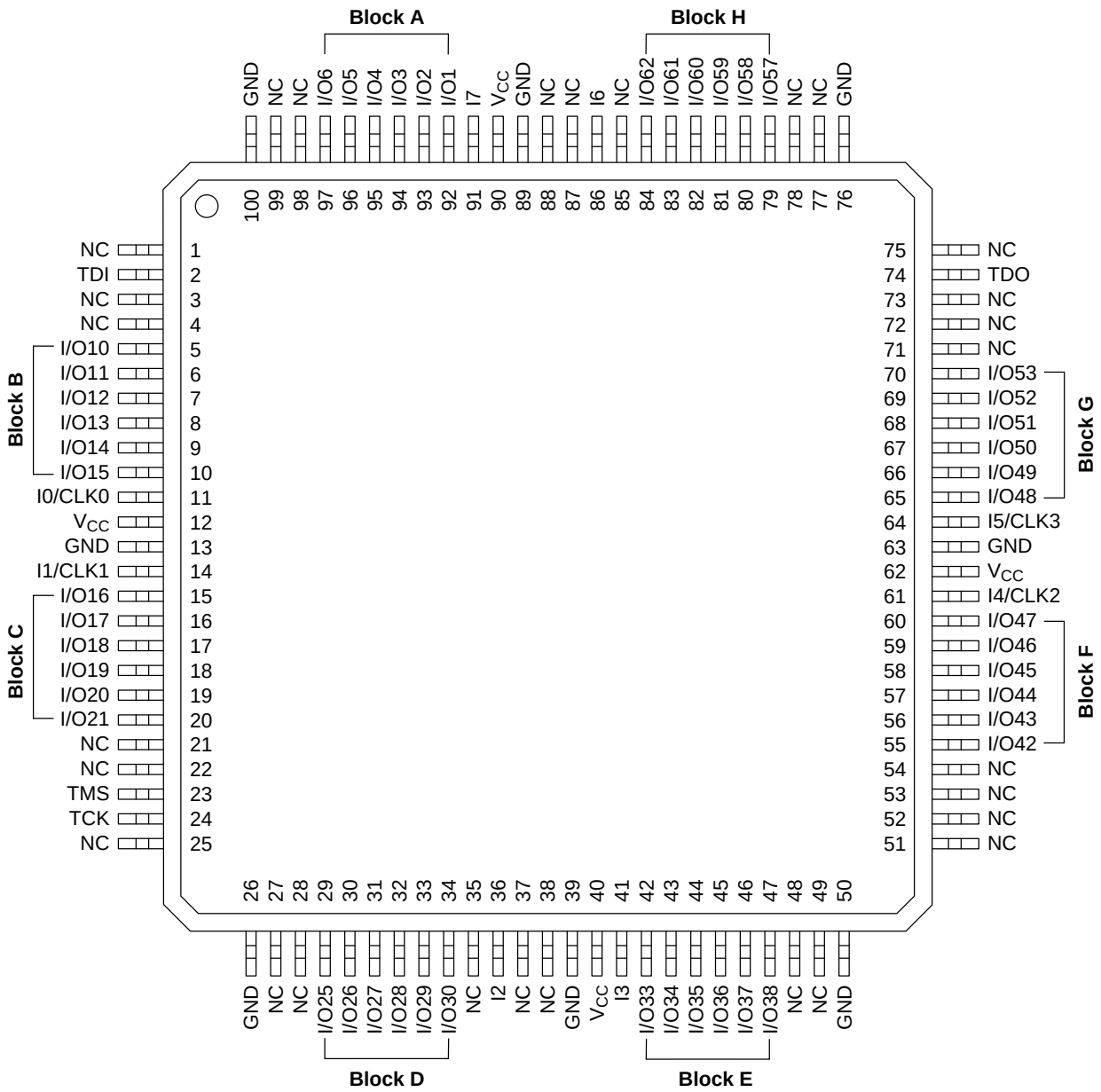
I/O = Input/Output

V_{CC} = Supply Voltage

CONNECTION DIAGRAM

Top View

100-Pin TQFP



Note:
Advance information for the M4(LV)-96.

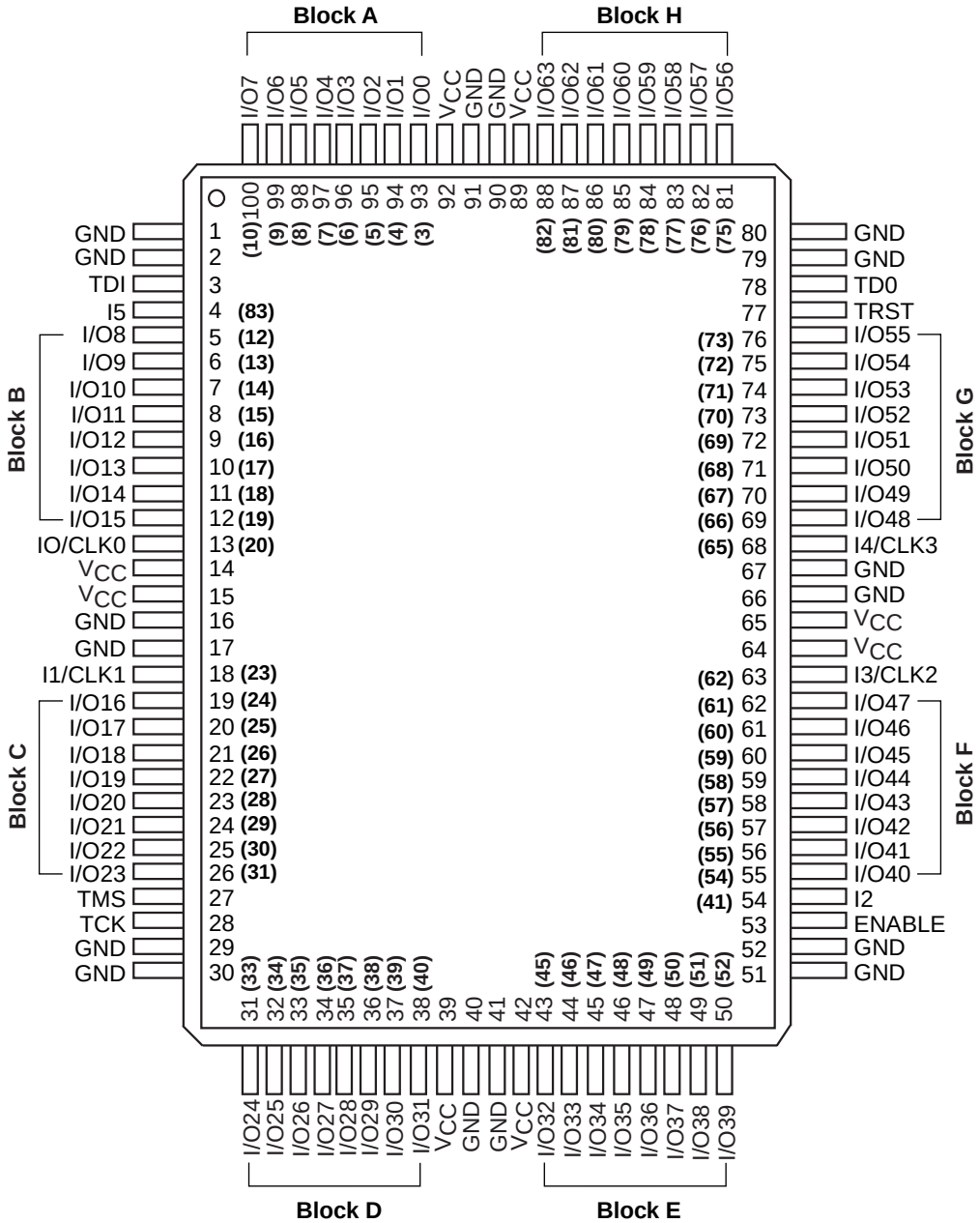
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
NC = No connect
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

CONNECTION DIAGRAM (M4(LV)-128)

Top View

100-Pin PQFP



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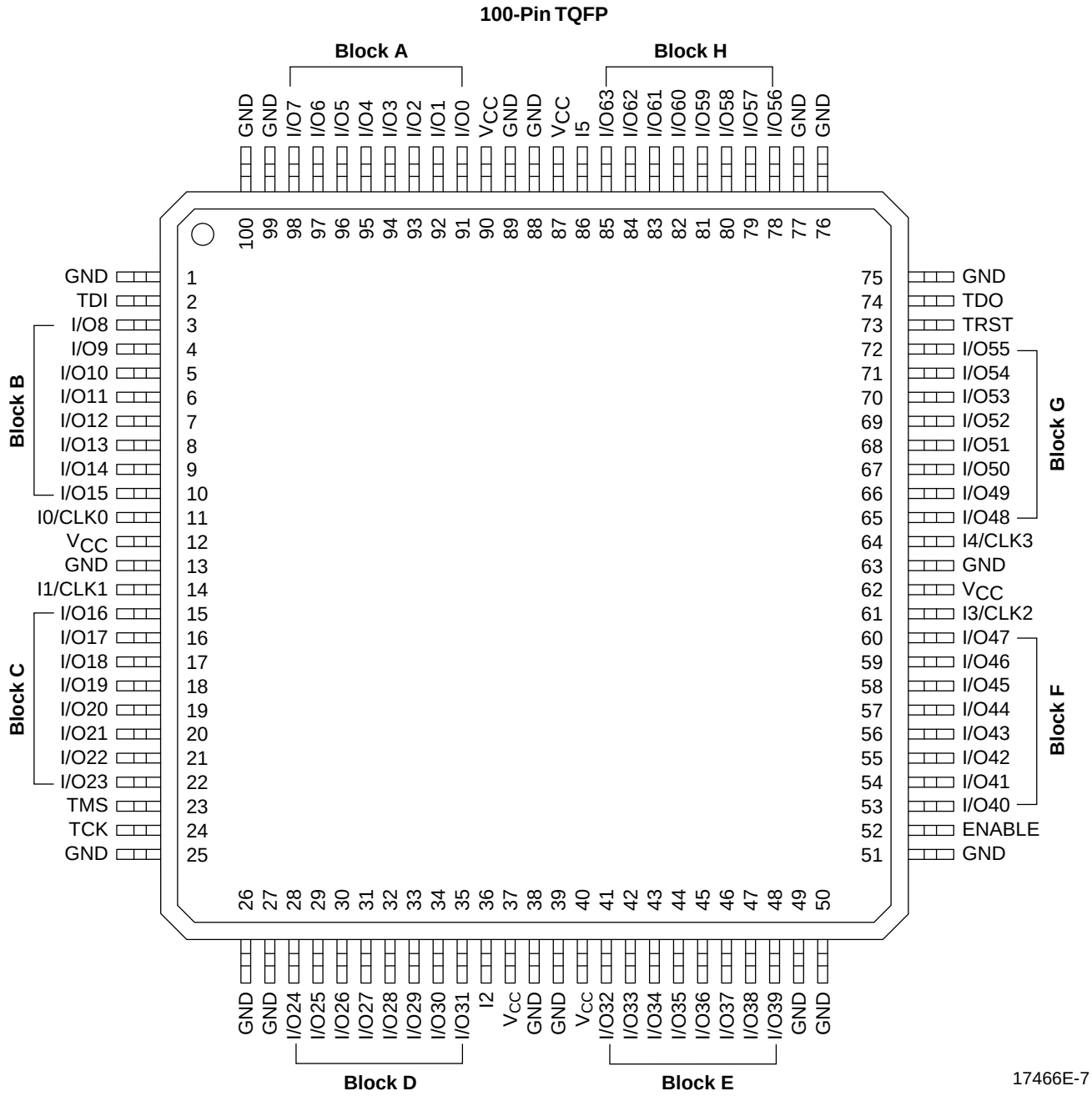
The numbers in parentheses reflect compatible pin numbers for 84-pin PLCC.

PIN DESIGNATIONS

I/CLK	=	Input or Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
V_{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out
TRST	=	Test Reset
ENABLE	=	Program

CONNECTION DIAGRAM (M4(LV)-128)

Top View



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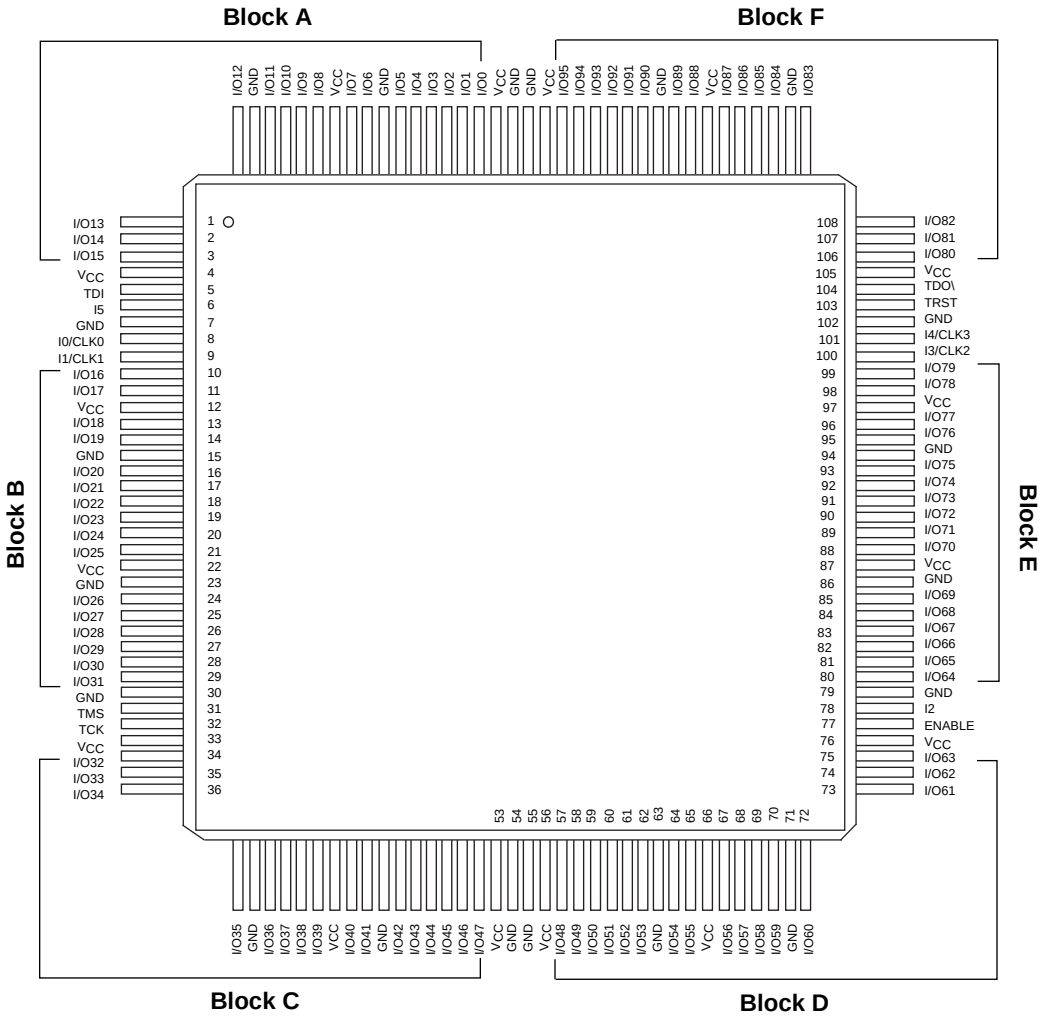
PIN DESIGNATIONS

CLK/I	=	Clock or Input	TDI	=	Test Data In
GND	=	Ground	TCK	=	Test Clock
I	=	Input	TMS	=	Test Mode Select
I/O	=	Input/Output	TDO	=	Test Data Out
V_{CC}	=	Supply Voltage	TRST	=	Test Reset
			ENABLE	=	Program

CONNECTION DIAGRAM (M4-96/96)

Top View

144-Pin PQFP



17466E-8

PIN DESIGNATIONS

CLK = Clock

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

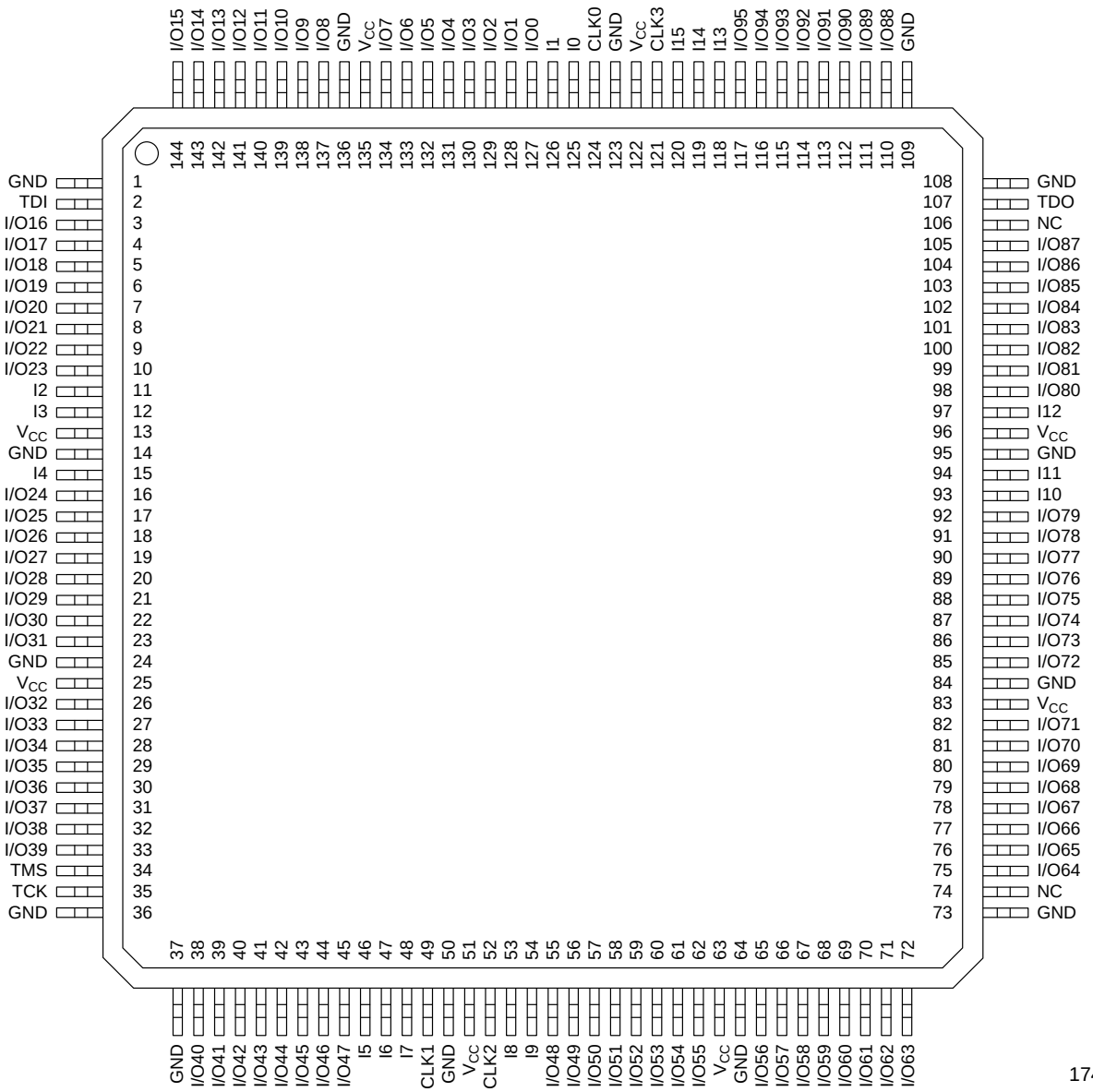
TRST = Test Reset

ENABLE = Program

CONNECTION DIAGRAM (M4(LV)-192)

Top View

144-Pin TQFP



17466E-9

Note:
Advance information for the M4(LV)-192.

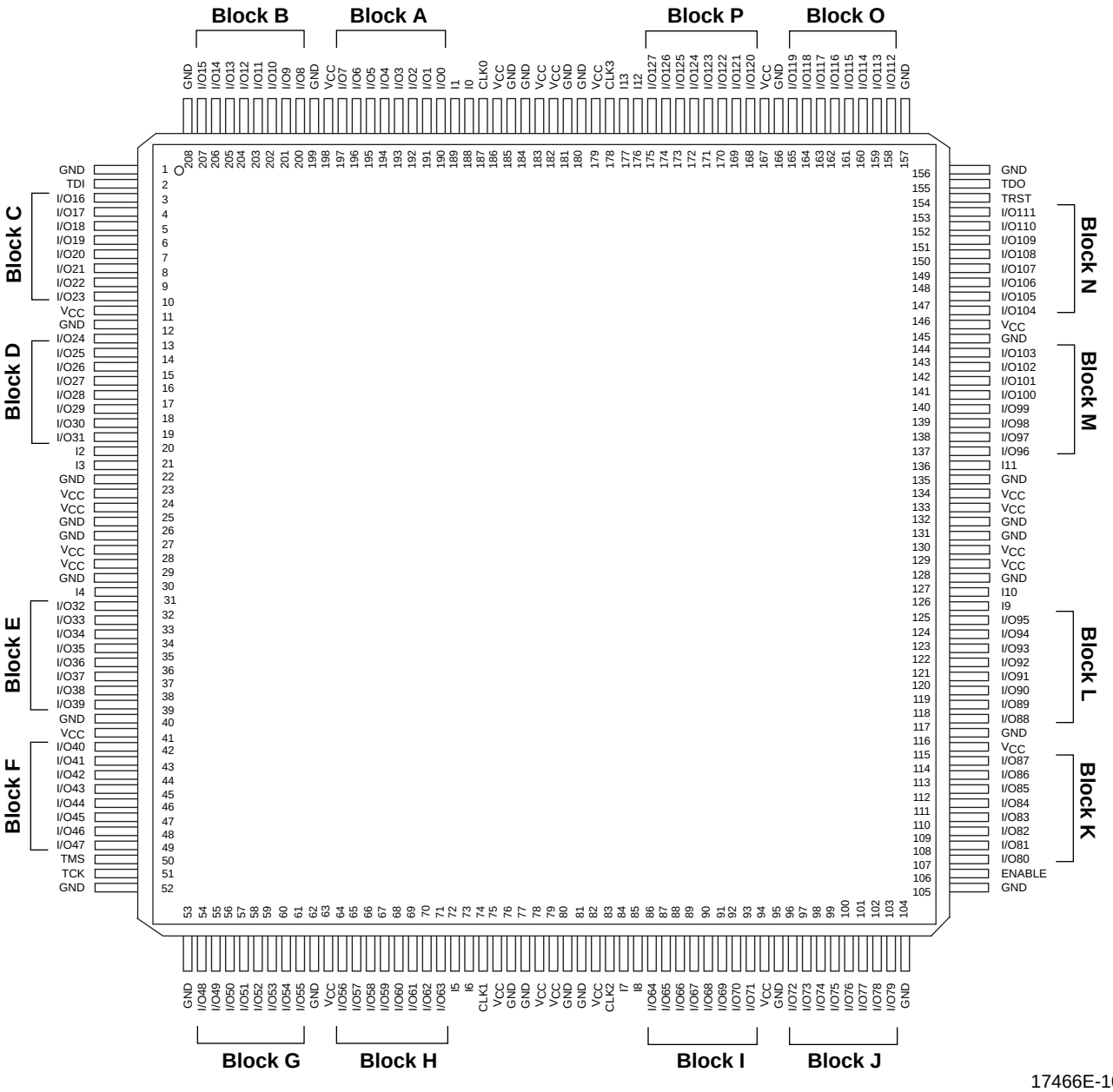
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

CONNECTION DIAGRAM (M4(LV)-256)

Top View

208-Pin PQFP



17466E-10

PIN DESIGNATIONS

CLK = Clock

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

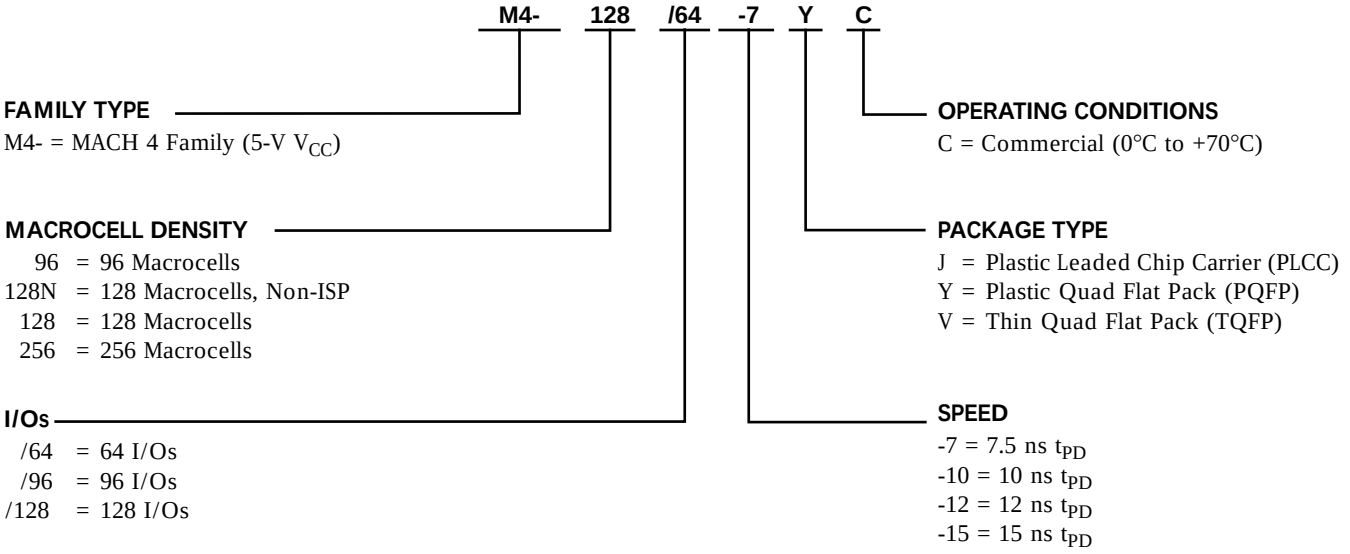
TRST = Test Reset

ENABLE = Program

ORDERING INFORMATION

Commercial Products

Vantis programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
M4-128N/64	-7, -10, -12, -15	JC
M4-96/96	-15	YC
M4-128/64	-7, -10, -12, -15	YC
M4-256/128	-10, -12, -15	
M4-128/64	-7, -10, -12, -15	VC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Commercial Products

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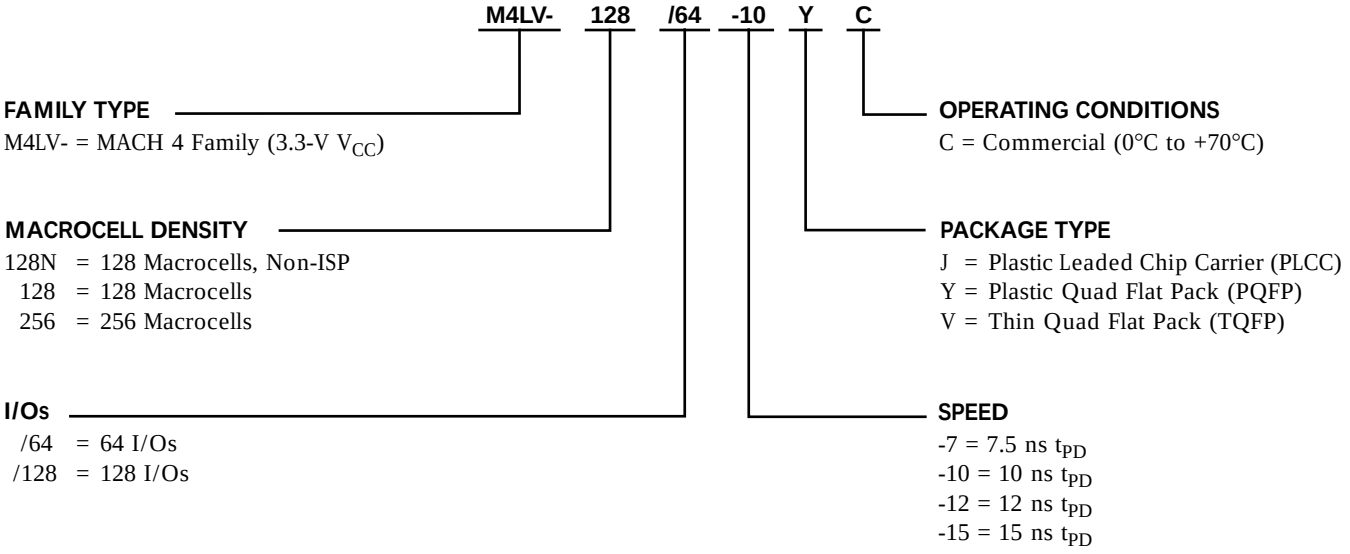


Valid Combinations		
M4LV-128N/64	-7, -10, -12, -15	JC
M4LV-128/64	-7, -10, -12, -15	YC
M4LV-256/128	-10, -12, -15	
M4LV-128/64	-7, -10, -12, -15	VC

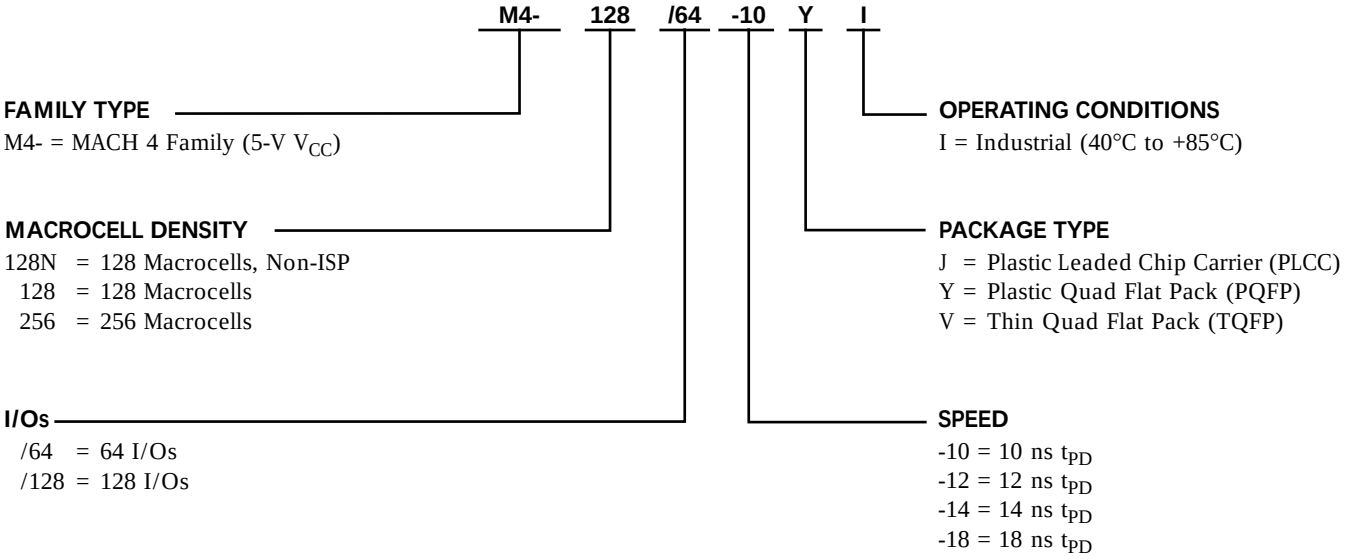
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Industrial Products

Vantis programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
M4-128N/64	-10, -12, -14, -18	JI
M4-128/64	-10, -12, -14, -18	YI
M4-256/128	-12, -14, -18	
M4-128/64	-10, -12, -14, -18	VI

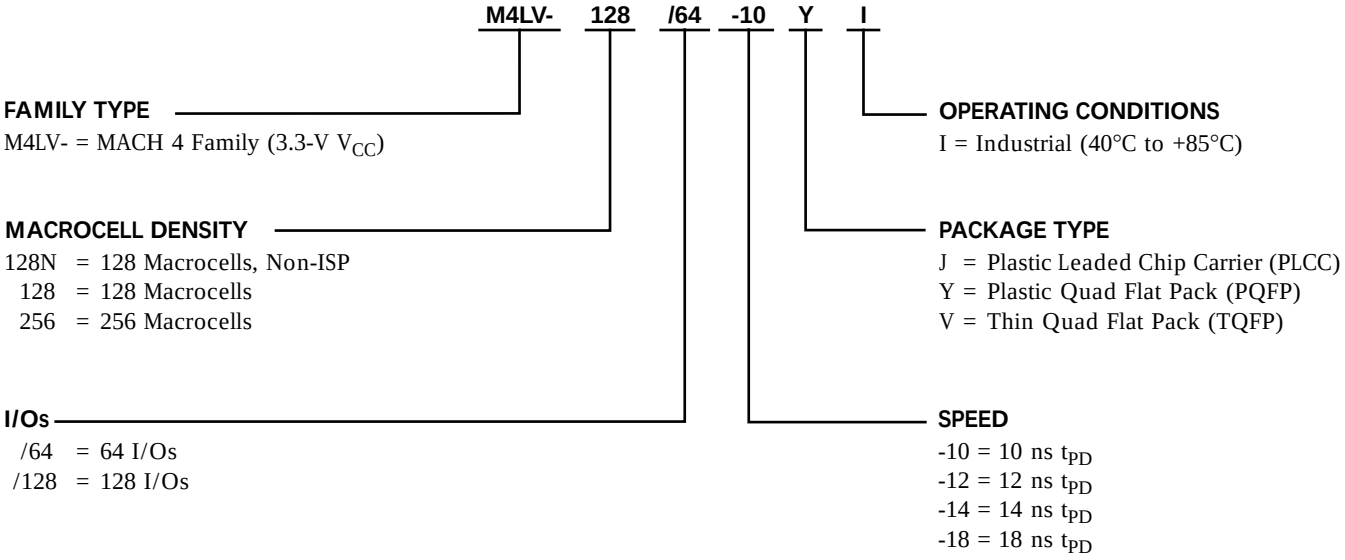
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Industrial Products

Vantis programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
M4LV-128N/64	-10, -12, -14, -18	JI
M4LV-128/64	-10, -12, -14, -18	YI
M4LV-256/128	-12, -14, -18	
M4LV-128/64	-10, -12, -14, -18	VI

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

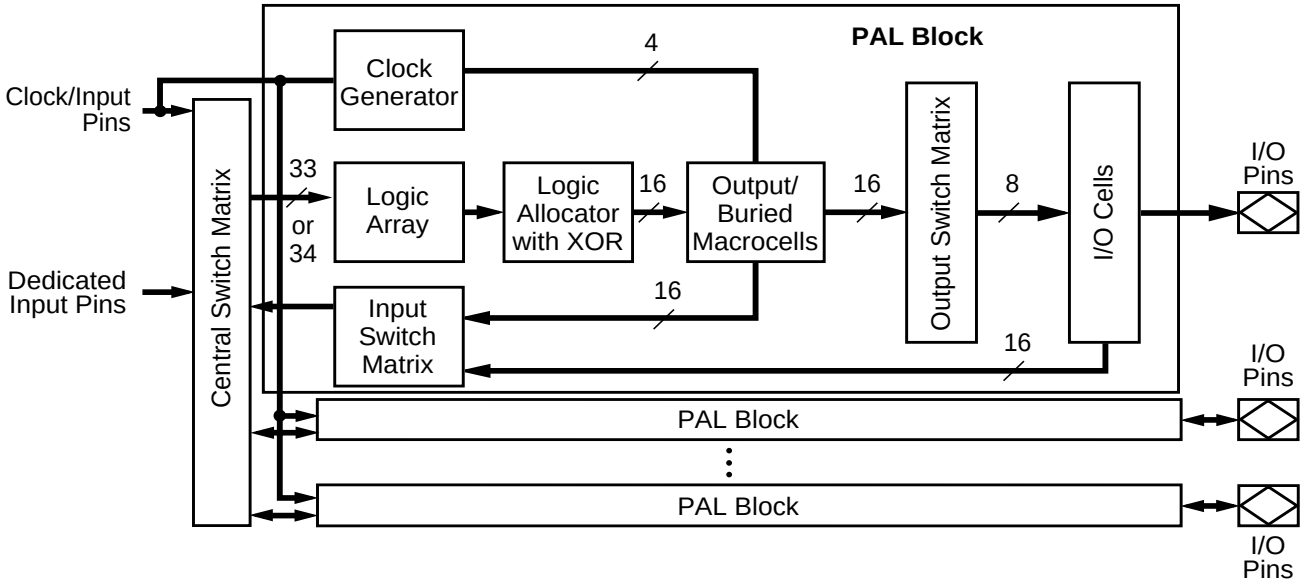
FUNCTIONAL DESCRIPTION

The fundamental architecture of the MACH 4 devices (Figure 1) consists of multiple optimized PAL blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks, and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of multiple devices.

Most pins are I/O pins that can be used as inputs, output, or bidirectional pins. There are some dedicated input pins, but all macrocells have internal feedback, allowing the pin to be used as an input if the macrocell signal is not needed externally.

The key to being able to make effective use of these devices lies in the interconnect schemes. Because of the programmable interconnections, the product term arrays have been decoupled from the central switch matrix; the macrocells have been decoupled from the product terms through the logic allocator; and the I/O pins have been decoupled from the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to place and route designs efficiently.

In a MACH 4 device, all signals incur the same delays, regardless of routing. Performance is design-independent, and is guaranteed by the SpeedLocking feature.



17466E-11

Figure 1. MACH 4 Block Diagram and PAL Block Structure

The PAL Blocks

The PAL blocks resemble independent PAL devices on the chip. This provides for logic functions that need the complete interconnect that a PAL device provides. PAL blocks communicate with each other through the central switch matrix.

Each PAL block consists of:

- a product-term array
- a logic allocator
- macrocells
- an output switch matrix
- I/O cells
- an input switch matrix
- a clock generator

The logic allocator distributes the product terms to the macrocells, as required by each individual design. The macrocell configures the signal largely by determining the storage characteristics. Macrocell signals are routed to I/O cells and the I/O pins by the output switch matrix. The I/O cells on the MACH 4 devices also allow for registered or latched inputs. The input switch matrix optimizes the routing of input signals into the central switch matrix.

The clock generator uses the four global clock inputs to generate a set of four clock signals available throughout the PAL block. Various combinations of clock signals in both true and complement form can be generated.

Each PAL block also contains an asynchronous reset product term and an asynchronous preset product term to be used for synchronous-mode macrocells. This allows synchronous flip-flops within a single PAL block to be initialized as a bank. Macrocells implemented in asynchronous mode are not affected by the PAL-block initialization.

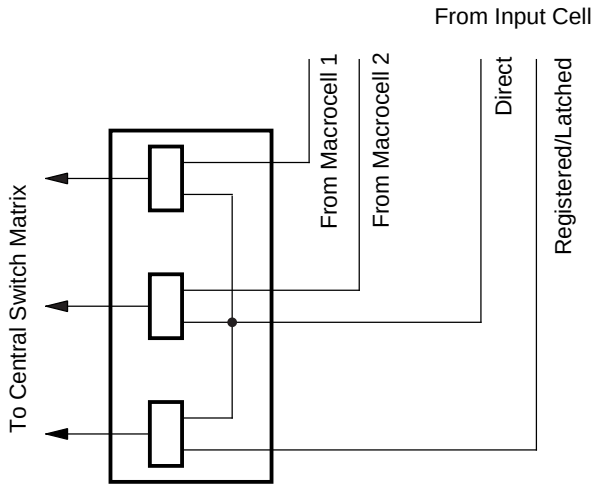
The Central Switch Matrix

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that only return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in the MACH 4 devices communicate with each other with consistent, predictable delays.

The central switch matrix makes a MACH 4 device more than just several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

The Input Switch Matrix

The input switch matrix (Figure 2) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.

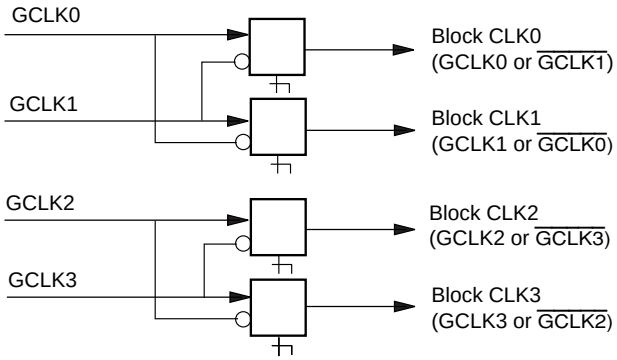


17466E-12

Figure 2. MACH 4 Input Switch Matrix

PAL Block Clock Generation

Each MACH 4 device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 3). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals; Table 1 lists the possible combinations.



17466E-13

Figure 3. PAL Block Clock Generator

Table 1. PAL Block Clock Combinations

Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{\text{GCLK1}}$	GCLK1	X	X
GCLK0	$\overline{\text{GCLK0}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK0}}$	X	X
X	X	GCLK2	GCLK3
X	X	$\overline{\text{GCLK3}}$	GCLK3
X	X	GCLK2	$\overline{\text{GCLK2}}$
X	X	$\overline{\text{GCLK3}}$	$\overline{\text{GCLK2}}$

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

Synchronous and Asynchronous Operation

The MACH 4 family can perform synchronous or asynchronous logic. Each individual cell can be programmed as synchronous or asynchronous, allowing unlimited “mixing and matching” of the two logic styles. The selection of synchronous or asynchronous mode affects the logic allocator and the macrocell, since product terms used for logic in the synchronous mode are used for control functions in the asynchronous mode.

The Product Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 2), and are provided in both true and complement forms for efficient logic implementation.

Table 2. PAL Block Inputs

Device	Number of Inputs to PAL Block
M4(LV)-32	33
M4(LV)-64	33
M4(LV)-96	33
M4(LV)-128	33
M4(LV)-192	33
M4(LV)-256	34

Because the number of product terms available for a given logic function is not fixed, the full sum of products is not realized in the array. The product terms drive the logic allocator, which allocates the appropriate number of product terms to generate the function.

The Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in “product term clusters.” The availability and distribution of product term clusters are automatically considered by the software as it places and routes functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over.

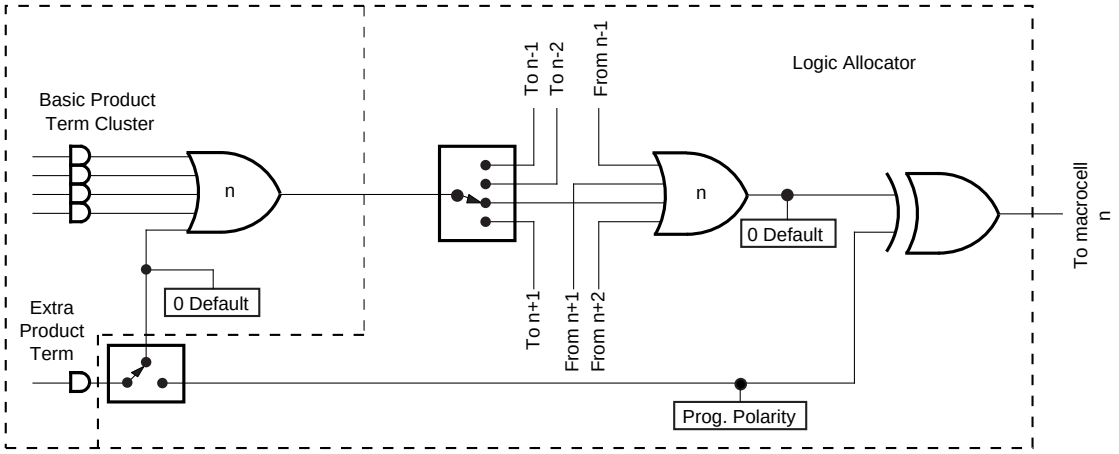
The logic allocator has two fundamental modes, depending on whether the macrocell is synchronous or asynchronous. The synchronous mode (Figure 4a) has a basic product term cluster of four product terms; the asynchronous mode (Figure 4b) has a basic cluster of two product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

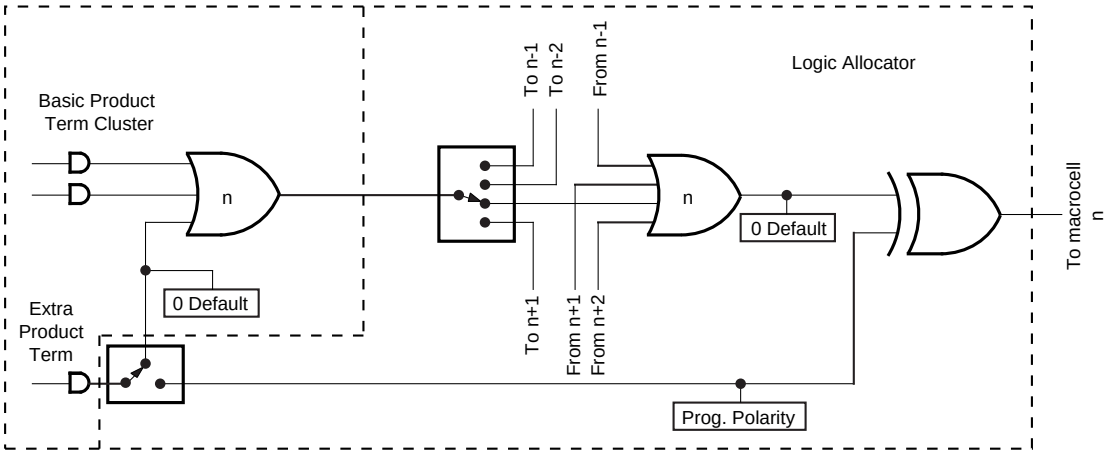
When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 5 and 6.

Table 3. Logic Allocator

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M_0	C_0, C_1, C_2	M_8	C_7, C_8, C_9, C_{10}
M_1	C_0, C_1, C_2, C_3	M_9	C_8, C_9, C_{10}, C_{11}
M_2	C_1, C_2, C_3, C_4	M_{10}	C_9, C_{10}, C_{11}, C_{12}
M_3	C_2, C_3, C_4, C_5	M_{11}	C_{10}, C_{11}, C_{12}, C_{13}
M_4	C_3, C_4, C_5, C_6	M_{12}	C_{11}, C_{12}, C_{13}, C_{14}
M_5	C_4, C_5, C_6, C_7	M_{13}	C_{12}, C_{13}, C_{14}, C_{15}
M_6	C_5, C_6, C_7, C_8	M_{14}	C_{13}, C_{14}, C_{15}
M_7	C_6, C_7, C_8, C_9	M_{15}	C_{14}, C_{15}



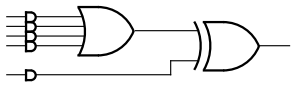
a. Synchronous Mode



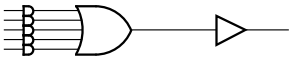
b. Asynchronous Mode

17466E-14

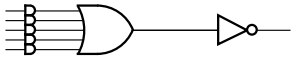
Figure 4. Logic Allocator. Configuration of cluster "n" set by mode of macrocell "n".



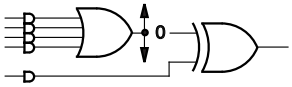
a. Basic cluster with XOR



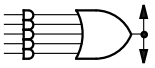
b. Extended cluster, active high



c. Extended cluster, active low



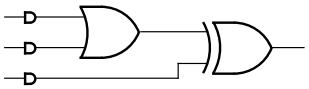
d. Basic cluster routed away; single-product-term, active high



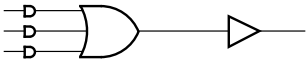
e. Extended cluster routed away

17466E-15

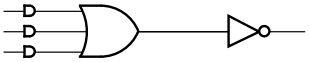
Figure 5. Logic Allocator Configurations: Synchronous Mode



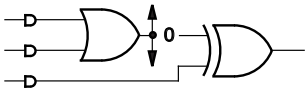
a. Basic cluster with XOR



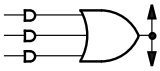
b. Extended cluster, active high



c. Extended cluster, active low



d. Basic cluster routed away; single-product-term, active high



e. Extended cluster routed away

17466E-16

Figure 6. Logic Allocator Configurations: Asynchronous Mode

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

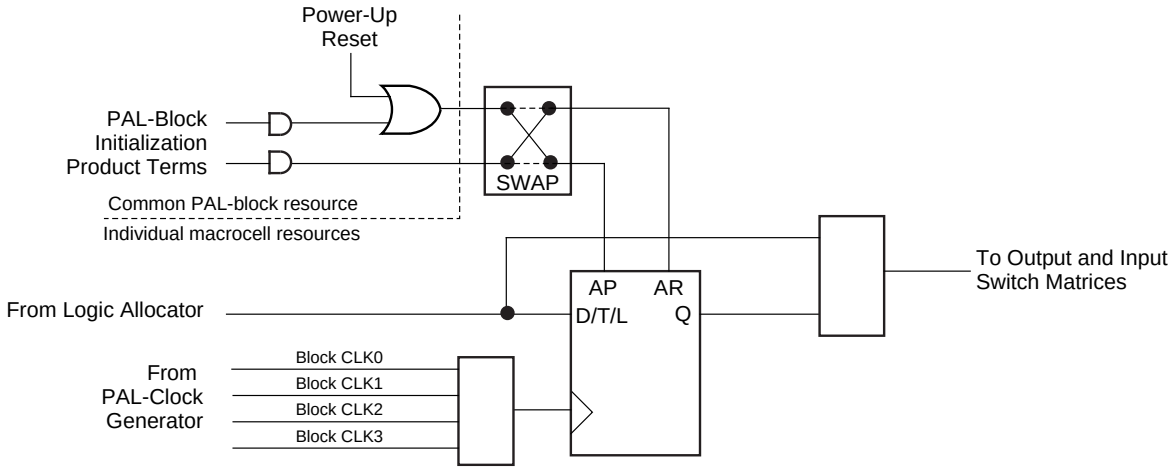
If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to

another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

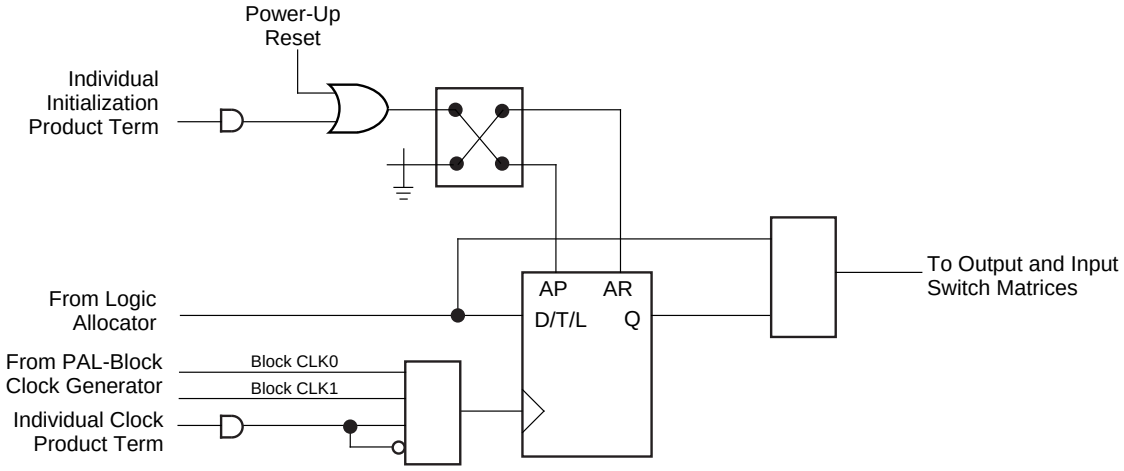
Product term clusters do not “wrap” around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available. Refer to the individual product data sheets for details.

The Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 7). The mode chosen only affects clocking and initialization in the macrocell.



a. Synchronous Mode



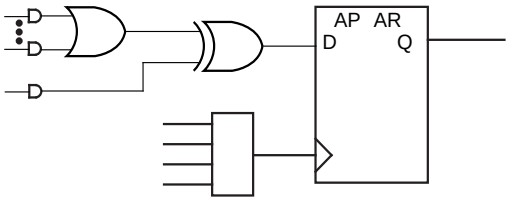
b. Asynchronous Mode

17466E-17

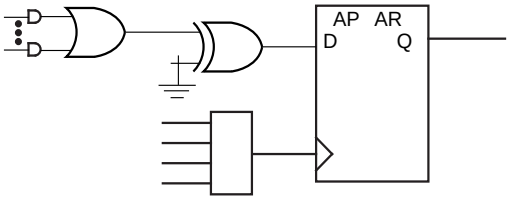
Figure 7. Macrocell

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

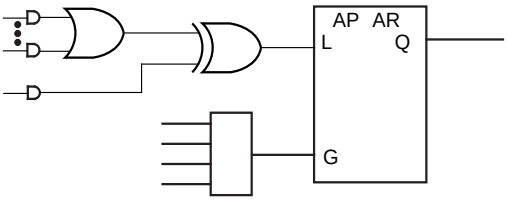
The flip-flop can be configured as a D-type, T-type, J-K, or S-R register or latch. The primary flip-flop configurations are shown in Figure 8, although others are possible. Flip-flop functionality is defined in Table 4. Note that a J-K latch is inadvisable, as it will cause oscillation if both J and K inputs are HIGH.



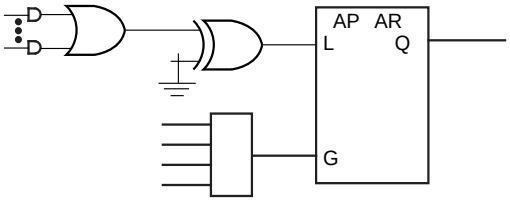
a. D-type with XOR



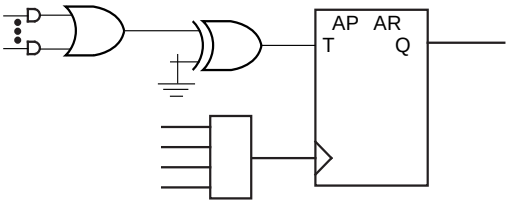
b. D-type with programmable D polarity



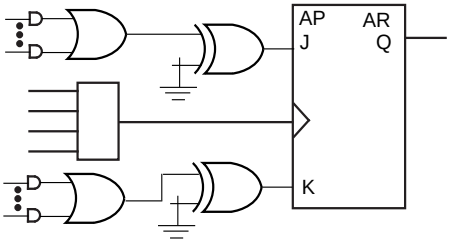
c. Latch with XOR



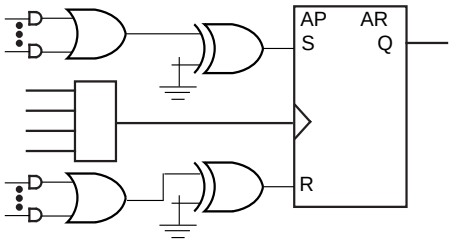
d. Latch with programmable polarity



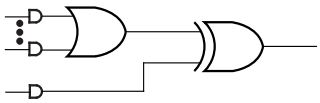
e. T-type with programmable T polarity



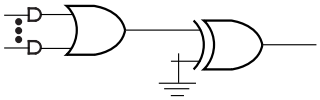
f. J-K with programmable J and K polarity



g. S-R with programmable S and R polarity



h. Combinatorial with XOR



i. Combinatorial with programmable polarity

17466E-18

Figure 8. Primary Macrocell Configurations

Table 4. Register/Latch Operation

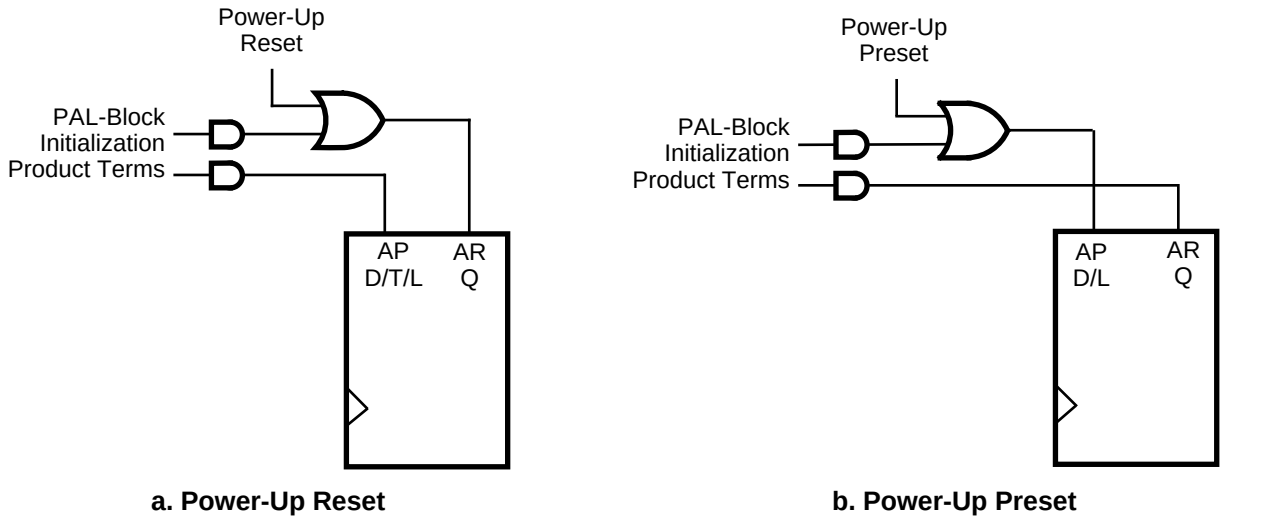
Configuration	Input(s)	CLK/LE*	Q+
D-type Register	D=X	0,1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ ↓	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\overline{Q}$
J-K Register	J=K=X	0,1, ↓ (↑)	Q
	J=0, K=0	↑ (↓)	Q
	J=0, K=1	↑ (↓)	0
	J=1, K=0	↑ (↓)	1
	J=1, K=1	↑ (↓)	$\overline{Q}$
S-R Register	S=R=X	0,1, O (↓)	Q
	S=0, R=0	↑ (↓)	Q
	S=0, R=1	↑ (↓)	0
	S=1, R=0	↑ (↓)	1
	S=1, R=1	↑ (↓)	Undefined
D-type Latch	D=X	1(0)	Q
	D=0	0(1)	0
	D=1	0(1)	1

**Polarity of CLK/LE can be programmed.*

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 9), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



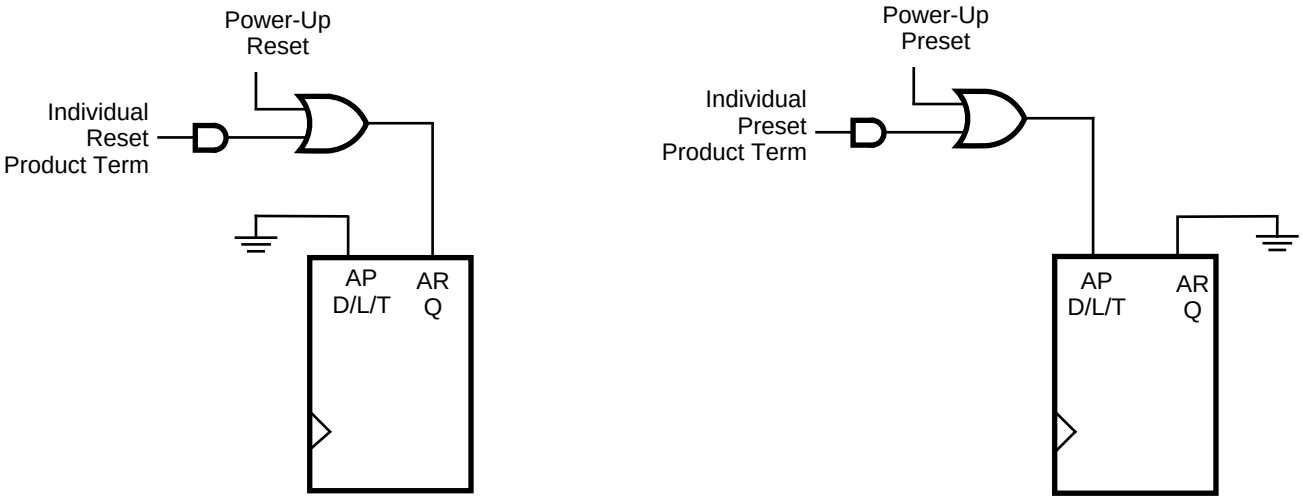
a. Power-Up Reset **b. Power-Up Preset**

17466E-19

Figure 9. Synchronous Mode Initialization Configurations

A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

In asynchronous mode (Figure 10), a single individual product term is provided for initialization. It can be selected to control reset or preset.



a. Reset **b. Preset**

17466E-20

Figure 10. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping selection feature affects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 5.

The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 5. Asynchronous Reset/Preset Operation

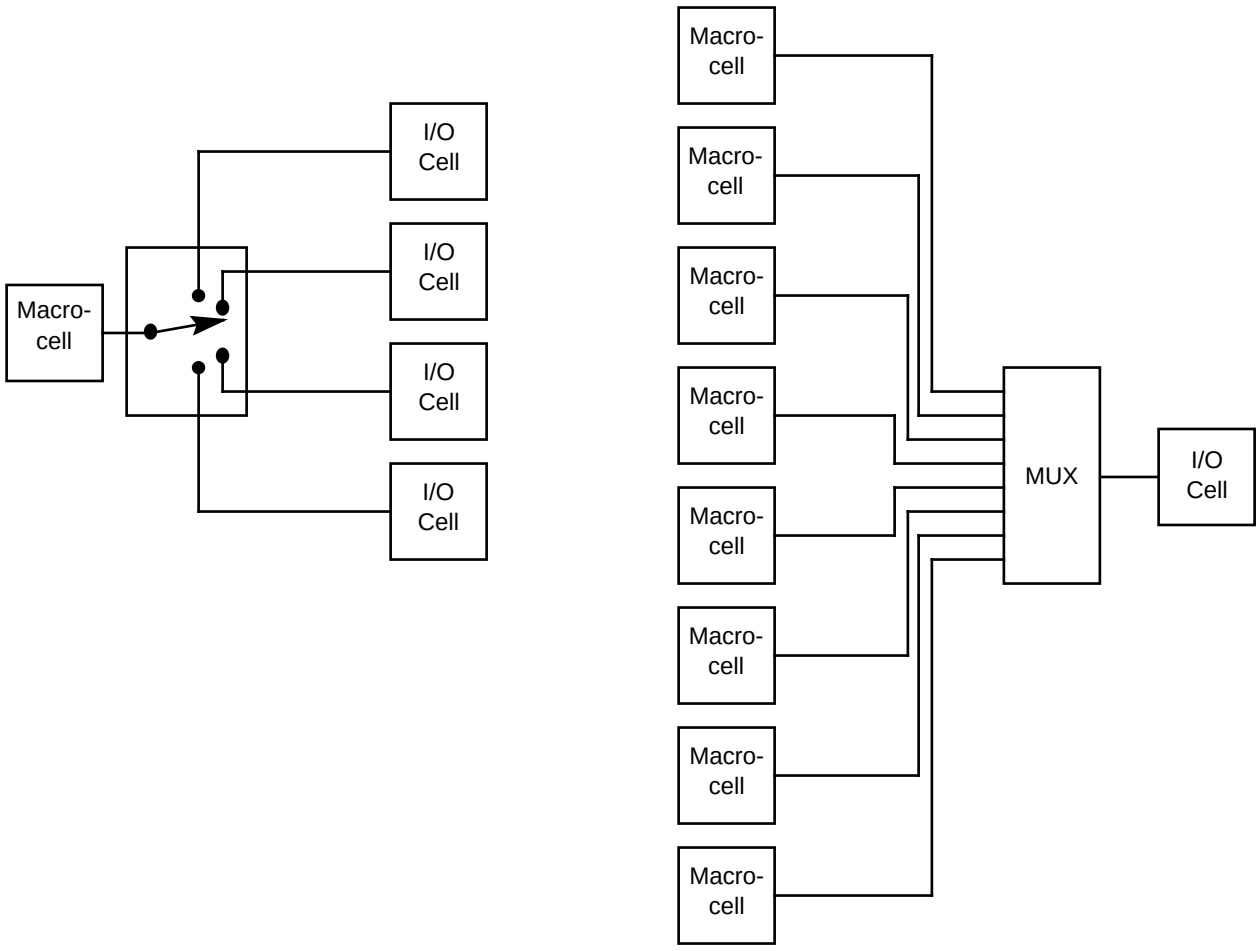
AR	AP	CLK/LE*	Q+
0	0	X	See Table 3
0	1	X	1
1	0	X	0
1	1	X	0

**Transparent latch is unaffected by AR, AP.*

The Output Switch Matrix

The output switch matrix allows macrocells to be connected to any of several I/O cells within a PAL Block. This provides high flexibility in determining pinout, and allows design changes that will not affect pinout.

In the MACH 4 devices, each PAL block has twice as many macrocells as I/O cells. The MACH 4 output switch matrix allows for half of the macrocells to drive I/O cells within a PAL block, in combinations according to Figure 11. Each I/O cell can choose from eight macrocells; each macrocell has a choice of four I/O cells.



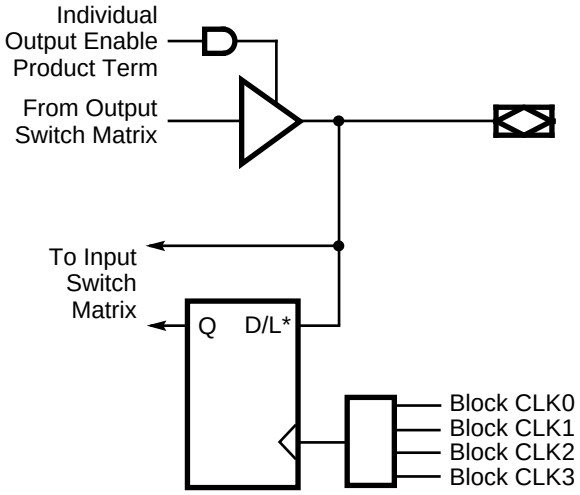
a. Macrocell drives one of 4 I/Os **b. I/O can choose one of 8 macrocells**

17466E-21

Figure 11. MACH 4 Output Switch Matrix

The I/O Cell

The I/O cell (Figure 12) simply consists of programmable output enable, a feedback path, and in the MACH 4 devices, a flip-flop. An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.



17466E-22

Figure 12. I/O Cell

The MACH 4 I/O cell contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as “time-domain-multiplexed” data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

Note that the flip-flop used in the MACH 4 I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

SpeedLocking for Guaranteed Fixed Timing

The MACH 4 architecture allows allocation of up to 20 product terms to an individual macrocell with the assistance of an XOR gate *without* incurring additional timing delays.

Using this architectural strength, the MACH 4 devices provide the industry's highest-speed and *only* fixed timing at both 3.3-V and 5-V supply voltages. This SpeedLocking feature delivers guaranteed fixed speed independent of logic path, routing resources, or design refits.

JTAG Boundary Scan Testability

All MACH 4 devices, except the M4(LV)-128N, have JTAG boundary scan cells built in. This allows functional testing of the device through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

5-V or 3.3-V In-System Programming

Another benefit from the JTAG circuitry that Vantis has derived is the ability to use the JTAG port for 5-V or 3.3-V in-system programming. This allows the device to be soldered to the board before

programming. Once the device is attached, the delicate PQFP or TQFP leads are protected from programming and testing operations that could potentially damage them. Programming and verification of the device is done serially, and it only requires the use of the Test Access Port. Use of the programming Enable pin (ENABLE) is optional.

Zero-Hold-Time Input Register

The MACH 4 devices have a zero-hold time (ZHT) fuse. This fuse controls the time delay associated with loading data into all I/O cell registers and latches in the MACH 4 devices.

When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized.

This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

Power-Down Mode

Each individual PAL block in the MACH 4 devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slightly slower than those in the non-low-power PAL block. This feature allows speed critical signal paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

Bus-Friendly Inputs and I/Os

The MACH 4 devices' inputs and I/Os feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state and pulls the voltage away from the input threshold voltage. At power-up, the Bus-Friendly latches are reset to a logic level "1." For an illustration of this configuration, please refer to the Input/Output Equivalent Schematics section.

Programmable Slew Rate

Each MACH 4 device I/O has an individually programmable output slew-rate control bit. Each output can be individually configured for the highest speed transition or for the lowest noise transition. In systems properly designed for high-speed applications, the fast slew-rate output option can be used to achieve the highest speed. However, the slower slew rate is more effective than the fast slew rate in keeping noise generation and ground bounce to the minimum level.

PCI Compliant

The MACH 4 devices with speed grades -7, -10 and -12 are compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The predictable timing of the MACH 4 devices ensures compliance with the PCI timing specifications independent of the logic design fitting.

Safe for Mixed Supply Voltage System Designs

The MACH 4 devices are safe for mixed supply voltage system designs. The 5-V device will not overdrive 3.3-V devices above the output voltage of 3.3 V, while it accepts inputs from other 3.3-V devices. The 3.3-V device will accept inputs up to 5.5 V. Thus, the MACH 4 devices provide easy-to-use mixed-voltage design capability.

Power-Up Reset/Preset

All flip-flops power up to a known state for predictable system initialization. The power-up value can be programmed through the initialization swapping selection feature. The V_{CC} rise must be monotonic and clock must be inactive until the reset delay time, 10 µs maximum, has elapsed.

Security Bit

A security bit is provided on the MACH 4 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. Preload and the JTAG circuitry can be used independently of the security bit, since a separate security bit is provided to disable these features. The bits can only be erased in conjunction with the array during an erase cycle.

Quality and Testability

The MACH devices offer a very high level of built-in quality. The fact that the device is erasable allows direct verification of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The MACH 4 devices, except the M4-96/96, are fabricated on Vantis' advanced electrically-erasable 0.35-µm (L_{eff}) CMOS technology. This provides the devices with performance and power consumption that are unmatched in the industry. The floating gate cells rely on Fowler-Nordheim tunnelling to charge the gate, and have long proven their endurance and reliability.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = 0°C to +70°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4		3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note1)

Parameter Symbol	Parameter Description				-7		-10		-12		-15		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				3	7.5	3	10	3	12	3	15	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	3.5		4		5		8		ns
				T-type	4.5		5		6		9		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				3.5		4		5		8		ns
t_{COA}	Product Term Clock to Output				4	9.5	4	12	4	14	4	18	ns
t_{WLA}	Product Term, Clock Width			LOW	4		5		8		9		ns
t_{WHA}				HIGH	4		5		8		9		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	74.0		62.5		52.6		38.5		MHz
				T-type	71.4		58.8		50.0		37		MHz
		Internal Feedback (f_{CNTA})		D-type	90.9		71.4		58.8		47.6		MHz
				T-type	83.3		66.7		55.6		45.4		MHz
		No Feedback (Note 3)	$1/(t_{WLA} + t_{WHA})$		125		100		62.5		55.6		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	5.5		6		7		10		ns
				T-type	6.5		7		8		11		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		0		ns
t_{COS}	Global Clock to Output				2	5.5	2	6.5	2	8	2	10	ns
t_{WLS}	Global Clock Width			LOW	3		5		6		6		ns
t_{WHS}				HIGH	3		5		6		6		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	90		80		66.7		50		MHz
				T-type	83.3		74.1		62.5		47.6		MHz
		Internal Feedback (f_{CNTS})		D-type	133		100		83.3		66.6		MHz
				T-type	117		90.9		76.9		62.5		MHz
		No Feedback (Note 3)	$1/(t_{WLS} + t_{WHS})$		166.7		100		83.3		88.3		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				4		4		5		8		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note1)

Parameter Symbol	Parameter Description		-7		-10		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{HLA}	Latch Data Hold Time Using Product Term Clock		4		4		5		8		ns
t_{GOA}	Product Term Gate to Output			11		13		16		19	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		4		5		6		9		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate		6		7		8		10		ns
t_{HLS}	Latch Data Hold Time Using Global Gate		0		0		0		0		ns
t_{GOS}	Gate to Output		6			7.5		10		11	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		5		6		6		ns
t_{ICO}	Input Register Clock to Combinatorial Output			14		15.5		18		20	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	7		8		9		15		
		T-type	8		9		10		16		
t_{WICL}	Input Register Clock Width	LOW	4.5		5		6		6		ns
t_{WICH}		HIGH	4.5		5		6		6		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	110		100		83.3		83.3		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			12		14		16		20	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			14		16		18		22	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		4		4		14		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		9		9		16		ns
t_{WIGL}	Input Latch Gate Width LOW		5		5		6		6		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			12		14		16		20	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		10		10		12		15		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		8		8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			12		14		16		20	ns
t_{APW}	Asynchronous Preset Width (Note 2)		10		10		12		15		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		8		8		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	9.5	2	10	2	12	2	15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	9.5	2	10	2	12	2	15	ns
Input Register with Standard-Hold-Time Option											
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			10		12		14		17	ns
t_{SIR}	Input Register Setup Time		2		2		2		2		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note1)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{HIR}	Input Register Hold Time	3		3		3		4		ns
t_{SIL}	Input Latch Setup Time	2		2		2		2		ns
t_{HIL}	Input Latch Hold Time	3		3		3		4		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	4		4		4		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	7		8		9		12		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		12		14		16		19	ns
Input Register with Zero-Hold-Time Option										
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		16		18		20		23	ns
t_{SIR}^{I}	Input Register Setup Time	6		6		6		6		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		6		6		6		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	11		13		16		16		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	12		15		18		18		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		18		20		22		25	ns
Power-Down Mode and Slow Slew Rate Option										
t_{LP}	Power-down mode delay adder. For macrocells in a power-down mode PAL block, this parameter must be added to: t_{PD}, t_{COA}, t_{SS}, t_{GOA}, t_{SLS}, t_{ICO}, t_{ICS}, t_{IGO}, t_{IGOL}, t_{IGSS}, t_{AR}, t_{ARR}, t_{AP}, t_{APR}, t_{EA}, t_{ER}, t_{PDL}, t_{SLLS}, t_{PDLL}		2.5		2.5		2.5		2.5	ns
t_{SLW}	Slow slew rate delay adder. For an output configured with slow slew rate option, this parameter must be added to: t_{PD}, t_{COA}, t_{COS}, t_{GOA}, t_{GOS}, t_{ICO}, t_{IGO}, t_{IGOL}, t_{AP}, t_{AR}, t_{PDL}, t_{PDLL}		2.5		2.5		2.5		2.5	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +4.5 V

DC Input Voltage . . . . . –0.5 V to 6.0 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = 0°C to +70°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 µA	V_{CC} – 0.2			V
			I_{OH} = –3.2 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 1)	I_{OL} = 100 µA			0.2	V
			I_{OL} = 24 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		–0.3		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				5	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–5	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				5	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				–5	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–15		–160	mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note1)

Parameter Symbol	Parameter Description				-7		-10		-12		-15		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				3	7.5	3	10	3	12	3	15	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	3.5		4		5		8		ns
				T-type	4.5		5		6		9		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				3.5		4		5		8		ns
t_{COA}	Product Term Clock to Output				4		4	12	4	14	4	18	ns
t_{WLA}	Product Term, Clock Width			LOW	4		5		8		9		ns
t_{WHA}				HIGH	4		5		8		9		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	74.0		62.5		52.6		38.5		MHz
				T-type	71.4		58.8		50.0		37		MHz
		Internal Feedback (f_{CNTA})		D-type	90.9		71.4		58.8		47.6		MHz
				T-type	83.3		66.7		55.6		45.4		MHz
		No Feedback (Note 3)	$1/(t_{WLA} + t_{WHA})$		125		100		62.5		55.6		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	5.5		6		7		10		ns
				T-type	6.5		7		8		11		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		0		ns
t_{COS}	Global Clock to Output				2	5.5	2	6.5	2	8	2	10	ns
t_{WLS}	Global Clock Width			LOW	3		5		6		6		ns
t_{WHS}				HIGH	3		5		6		6		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	90		80		66.7		50		MHz
				T-type	83.3		74.1		62.5		47.6		MHz
		Internal Feedback (f_{CNTS})		D-type	133		100		83.3		66.6		MHz
				T-type	117		90.9		76.9		62.5		MHz
		No Feedback (Note 3)	$1/(t_{WLS} + t_{WHS})$		166.7		100		83.3		88.3		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				4		4		5		8		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note1)

Parameter Symbol	Parameter Description		-7		-10		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{HLA}	Latch Data Hold Time Using Product Term Clock		4		4		5		8		ns
t_{GOA}	Product Term Gate to Output			11		13		16		19	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		4		5		6		9		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate		6		7		8		10		ns
t_{HLS}	Latch Data Hold Time Using Global Gate		0		0		0		0		ns
t_{GOS}	Gate to Output		6			7.5		10		11	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		5		6		6		ns
t_{ICO}	Input Register Clock to Combinatorial Output		14			15.5		18		20	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	7		8		9		15		
		T-type	8		9		10		16		
t_{WICL}	Input Register Clock Width	LOW	4.5		5		6		6		ns
t_{WICH}		HIGH	4.5		5		6		6		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	110		100		83.3		83.3		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			12		14		16		20	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			14		16		18		22	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		4		4		14		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		9		9		16		ns
t_{WIGL}	Input Latch Gate Width LOW		5		5		6		6		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			12		14		16		20	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		10		10		12		15		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		8		8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			12		14		16		20	ns
t_{APW}	Asynchronous Preset Width (Note 2)		10		10		12		15		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		8		8		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	9.5	2	10	2	12	2	15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	9.5	2	10	2	12	2	15	ns
Input Register with Standard-Hold-Time Option											
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			10		12		14		17	ns
t_{SIR}	Input Register Setup Time		2		2		2		2		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note1)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{HIR}	Input Register Hold Time	3		3		3		4		ns
t_{SIL}	Input Latch Setup Time	2		2		2		2		ns
t_{HIL}	Input Latch Hold Time	3		3		3		4		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	4		4		4		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	7		8		9		12		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches	12			14		16		19	ns
Input Register with Zero-Hold-Time Option										
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		16		18		20		23	ns
t_{SIR}^{I}	Input Register Setup Time	6		6		6		6		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		6		6		6		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	11		13		16		16		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	12		15		18		18		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		18		20		22		25	ns
Power-Down Mode and Slow Slew Rate Option										
t_{LP}	Power-down mode delay adder. For macrocells in a power-down mode PAL block, this parameter must be added to: t_{PD}, t_{COA}, t_{SS}, t_{GOA}, t_{SLS}, t_{ICO}, t_{ICS}, t_{IGO}, t_{IGOL}, t_{IGSS}, t_{AR}, t_{ARR}, t_{AP}, t_{APR}, t_{EA}, t_{ER}, t_{PDL}, t_{SLLS}, t_{PDLL}		2.5		2.5		2.5		2.5	ns
t_{SLW}	Slow slew rate delay adder. For an output configured with slow slew rate option, this parameter must be added to: t_{PD}, t_{COA}, t_{COS}, t_{GOA}, t_{GOS}, t_{ICO}, t_{IGO}, t_{IGOL}, t_{AP}, t_{AR}, t_{PDL}, t_{PDLL}		2.5		2.5		2.5		2.5	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = –40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.50 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4		3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note1)

Parameter Symbol	Parameter Description				-10		-12		-14		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				3	10	3	12	3	14	3	18	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	4		5		8		10		ns
				T-type	5		6		9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				4		5		8		10		ns
t_{COA}	Product Term Clock to Output				4	12	4	14	4	18	4	20	ns
t_{WLA}	Product Term, Clock Width			LOW	5		8		9		10		ns
t_{WHA}				HIGH	5		8		9		10		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	62.5		52.6		38.5		33.3		MHz
				T-type	58.8		50.0		37		32.2		MHz
		Internal Feedback (f_{CNTA})		D-type	71.4		58.8		47.6		35.7		MHz
				T-type	66.7		55.6		45.4		34.4		MHz
		No Feedback (Note 3)	$1/(t_{WLA} + t_{WHA})$		100		62.5		55.6		50.0		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	6		7		10		12		ns
				T-type	7		8		11		13		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		0		ns
t_{COS}	Global Clock to Output				2	6.5	2	8	2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	5		6		6		7		ns
t_{WHS}				HIGH	5		6		6		7		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	80		66.7		50		41.7		MHz
				T-type	74.1		62.5		47.6		40.0		MHz
		Internal Feedback (f_{CNTS})		D-type	100		83.3		66.6		58.8		MHz
				T-type	90.9		76.9		62.5		55.5		MHz
		No Feedback (Note 3)	$1/(t_{WLS} + t_{WHS})$		100		83.3		88.3		71.4		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				4		5		8		10		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note1)

Parameter Symbol	Parameter Description		-10		-12		-14		-18		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{HLA}	Latch Data Hold Time Using Product Term Clock		4		5		8		10		ns
t_{GOA}	Product Term Gate to Output			13		16		19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		6		9		11		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate		7		8		10		12		ns
t_{HLS}	Latch Data Hold Time Using Global Gate		0		0		0		0		ns
t_{GOS}	Gate to Output			7.5		10		11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		6		6		7		ns
t_{ICO}	Input Register Clock to Combinatorial Output			15.5		18		20		22	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	8		9		15		17		
		T-type	9		10		16		18		
t_{WICL}	Input Register Clock Width	LOW	5		6		6		7		ns
t_{WICH}		HIGH	5		6		6		7		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	100		83.3		83.3		71.4		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			14		16		20		22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			16		18		22		24	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		4		14		16		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		9		16		18		ns
t_{WIGL}	Input Latch Gate Width LOW		5		6		6		7		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			14		16		20		22	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		10		12		15		17		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		8		10		15		17		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			14		16		20		22	ns
t_{APW}	Asynchronous Preset Width (Note 2)		10		12		15		17		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		8		15		17		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	10	2	12	2	15	2	17	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	10	2	12	2	15	2	17	ns
Input Register with Standard-Hold-Time Option											
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			12		14		17		20	ns
t_{SIR}	Input Register Setup Time		2		2		2		2		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note1)

Parameter Symbol	Parameter Description	-10		-12		-14		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{HIR}	Input Register Hold Time	3		3		4		4		ns
t_{SIL}	Input Latch Setup Time	2		2		2		2		ns
t_{HIL}	Input Latch Hold Time	3		3		4		4		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	4		4		4		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	8		9		12		15		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		14		16		19		22	ns
Input Register with Zero-Hold-Time Option										
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		18		20		23		26	ns
t_{SIR}^{I}	Input Register Setup Time	6		6		6		6		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		6		6		6		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	13		16		16		16		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	15		18		18		18		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		20		22		25		27	ns
Power-Down Mode and Slow Slew Rate Option										
t_{LP}	Power-down mode delay adder. For macrocells in a power-down mode PAL block, this parameter must be added to: t_{PD}, t_{COA}, t_{SS}, t_{GOA}, t_{SLS}, t_{ICO}, t_{ICS}, t_{IGO}, t_{IGOL}, t_{IGSS}, t_{AR}, t_{ARR}, t_{AP}, t_{APR}, t_{EA}, t_{ER}, t_{PDL}, t_{SLLS}, t_{PDLL}		2.5		2.5		2.5		2.5	ns
t_{SLW}	Slow slew rate delay adder. For an output configured with slow slew rate option, this parameter must be added to: t_{PD}, t_{COA}, t_{COS}, t_{GOA}, t_{GOS}, t_{ICO}, t_{IGO}, t_{IGOL}, t_{AP}, t_{AR}, t_{PDL}, t_{PDLL}		2.5		2.5		2.5		2.5	ns

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +4.5 V

DC Input Voltage . . . . . –0.5 V to 6.0 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = –40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 µA	V_{CC} – 0.2			V
			I_{OH} = –3.2 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)	I_{OL} = 100 µA			0.2	V
			I_{OL} = 24 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		–0.3		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				5	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–5	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				5	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				–5	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–15		–160	mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note1)

Parameter Symbol	Parameter Description				-10		-12		-14		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				3	10	3	12	3	14	3	18	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	4		5		8		10		ns
				T-type	5		6		9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				4		5		8		10		ns
t_{COA}	Product Term Clock to Output				4	12	4	14	4	18	4	20	ns
t_{WLA}	Product Term, Clock Width			LOW	5		8		9		10		ns
t_{WHA}				HIGH	5		8		9		10		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	62.5		52.6		38.5		33.3		MHz
				T-type	58.8		50.0		37		32.2		MHz
		Internal Feedback (f_{CNTA})		D-type	71.4		58.8		47.6		35.7		MHz
				T-type	66.7		55.6		45.4		34.4		MHz
		No Feedback (Note 3)	$1/(t_{WLA} + t_{WHA})$		100		62.5		55.6		50.0		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	6		7		10		12		ns
				T-type	7		8		11		13		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		0		ns
t_{COS}	Global Clock to Output				2	6.5	2	8	2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	5		6		6		7		ns
t_{WHS}				HIGH	5		6		6		7		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	80		66.7		50		41.7		MHz
				T-type	74.1		62.5		47.6		40.0		MHz
		Internal Feedback (f_{CNTS})		D-type	100		83.3		66.6		58.8		MHz
				T-type	90.9		76.9		62.5		55.5		MHz
		No Feedback (Note 3)	$1/(t_{WLS} + t_{WHS})$		100		83.3		88.3		71.4		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				4		5		8		10		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note1)

Parameter Symbol	Parameter Description		-10		-12		-14		-18		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{HLA}	Latch Data Hold Time Using Product Term Clock		4		5		8		10		ns
t_{GOA}	Product Term Gate to Output			13		16		19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		6		9		11		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate		7		8		10		12		ns
t_{HLS}	Latch Data Hold Time Using Global Gate		0		0		0		0		ns
t_{GOS}	Gate to Output			7.5		10		11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		6		6		7		ns
t_{ICO}	Input Register Clock to Combinatorial Output			15.5		18		20		22	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	8		9		15		17		
		T-type	9		10		16		18		
t_{WICL}	Input Register Clock Width	LOW	5		6		6		7		ns
t_{WICH}		HIGH	5		6		6		7		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	100		83.3		83.3		71.4		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			14		16		20		22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			16		18		22		24	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		4		14		16		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		9		16		18		ns
t_{WIGL}	Input Latch Gate Width LOW		5		6		6		7		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			14		16		20		22	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		10		12		15		17		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		8		10		15		17		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			14		16		20		22	ns
t_{APW}	Asynchronous Preset Width (Note 2)		10		12		15		17		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		8		15		17		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	10	2	12	2	15	2	17	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	10	2	12	2	15	2	17	ns
Input Register with Standard-Hold-Time Option											
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			12		14		17		20	ns
t_{SIR}	Input Register Setup Time		2		2		2		2		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note1)

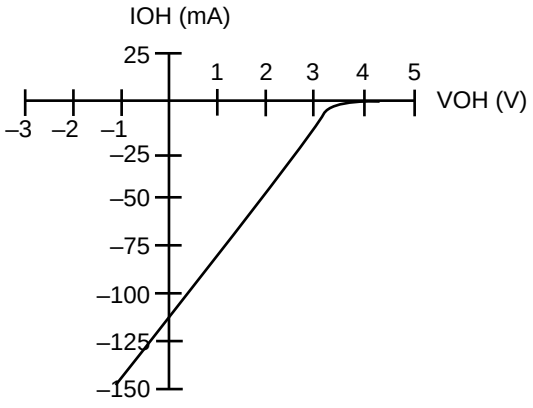
Parameter Symbol	Parameter Description	-10		-12		-14		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{HIR}	Input Register Hold Time	3		3		4		4		ns
t_{SIL}	Input Latch Setup Time	2		2		2		2		ns
t_{HIL}	Input Latch Hold Time	3		3		4		4		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	4		4		4		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	8		9		12		15		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		14		16		19		22	ns
Input Register with Zero-Hold-Time Option										
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		18		20		23		26	ns
t_{SIR}^{I}	Input Register Setup Time	6		6		6		6		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		6		6		6		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	13		16		16		16		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	15		18		18		18		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		20		22		25		27	ns
Power-Down Mode and Slow Slew Rate Option										
t_{LP}	Power-down mode delay adder. For macrocells in a power-down mode PAL block, this parameter must be added to: t_{PD}, t_{COA}, t_{SS}, t_{GOA}, t_{SLS}, t_{ICO}, t_{ICS}, t_{IGO}, t_{IGOL}, t_{IGSS}, t_{AR}, t_{ARR}, t_{AP}, t_{APR}, t_{EA}, t_{ER}, t_{PDL}, t_{SLLS}, t_{PDLL}		2.5		2.5		2.5		2.5	ns
t_{SLW}	Slow slew rate delay adder. For an output configured with slow slew rate option, this parameter must be added to: t_{PD}, t_{COA}, t_{COS}, t_{GOA}, t_{GOS}, t_{ICO}, t_{IGO}, t_{IGOL}, t_{AP}, t_{AR}, t_{PDL}, t_{PDLL}		2.5		2.5		2.5		2.5	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

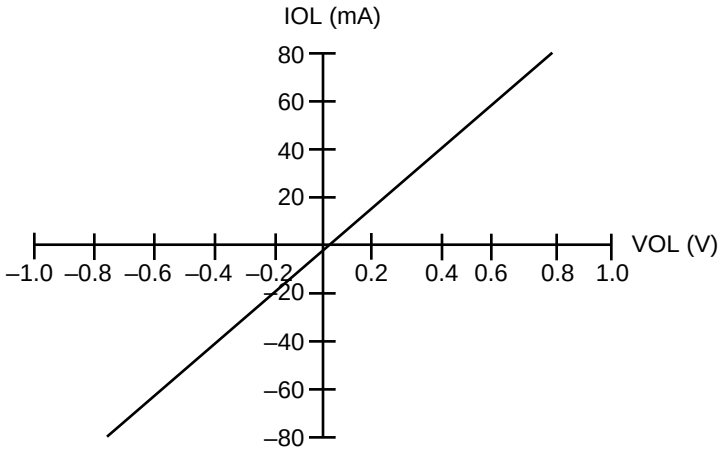
TYPICAL CURRENT vs. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5 V or 3.3 V, T_A = 25°C



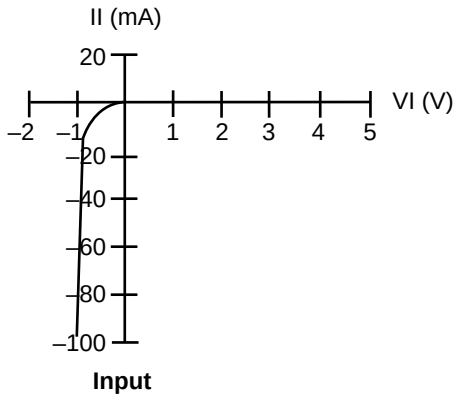
Output, HIGH

17466E-23



Output, LOW

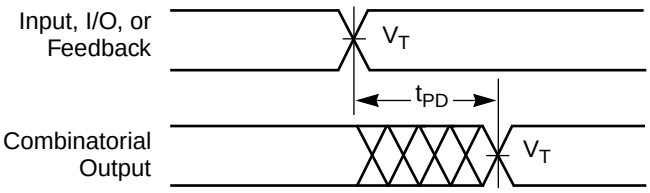
17466E-24



Input

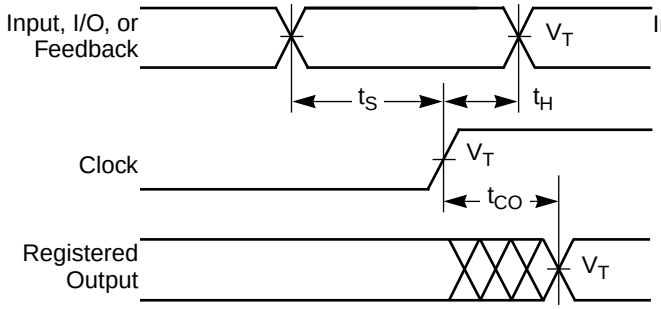
17466E-25

SWITCHING WAVEFORMS



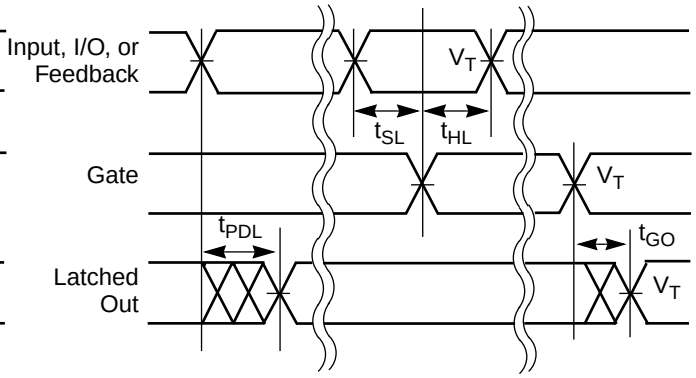
17466E-26

Combinatorial Output



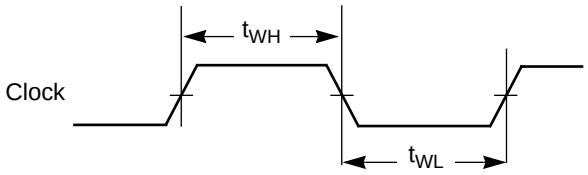
17466E-27

Registered Output



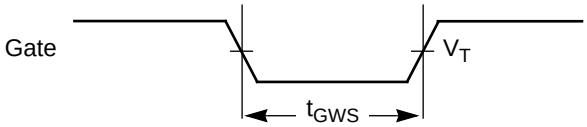
17466E-28

Latched Output



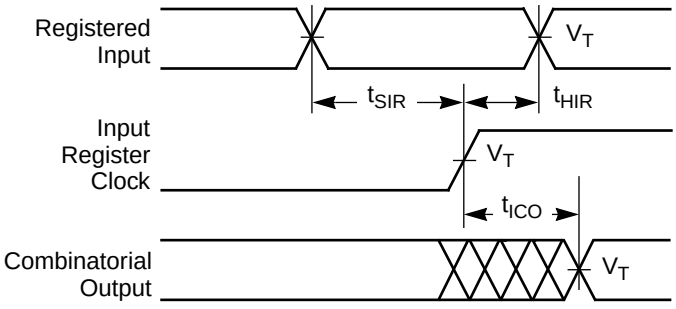
17466E-29

Clock Width



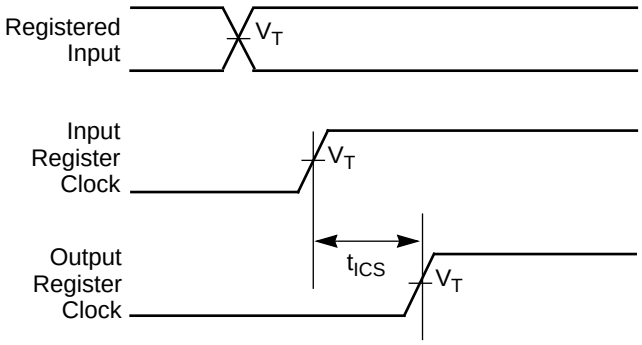
17466E-30

Gate Width



17466E-31

Registered Input



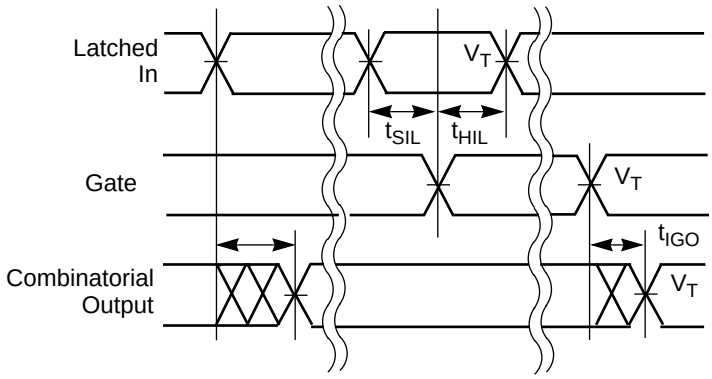
17466E-32

Input Register to Output Register Setup

Notes:

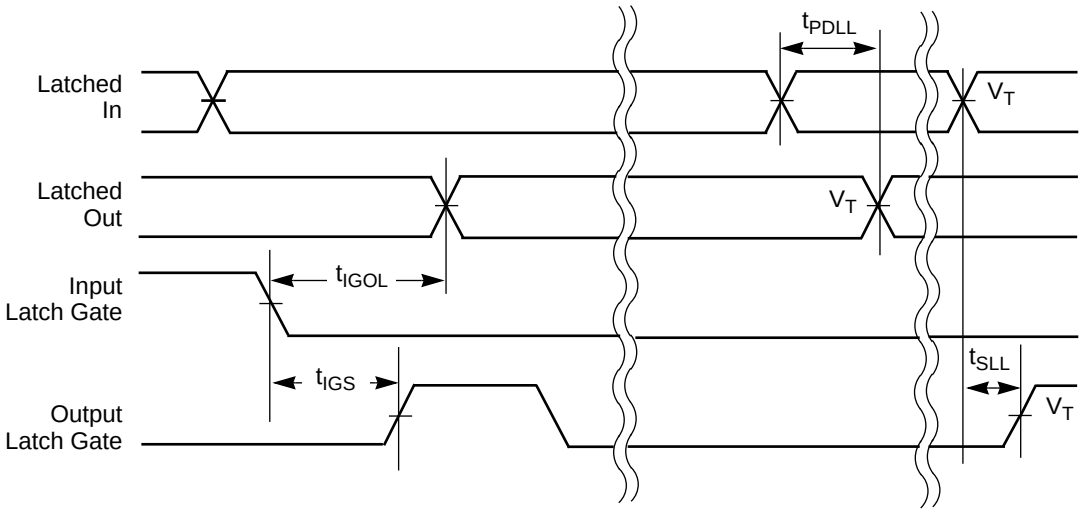
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



17466E-33

Latched Input



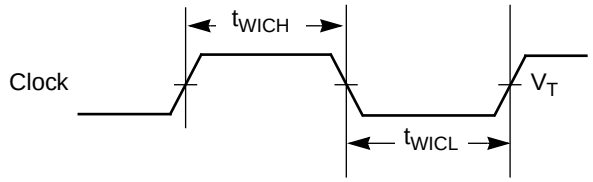
17466E-34

Latched Input and Output

Notes:

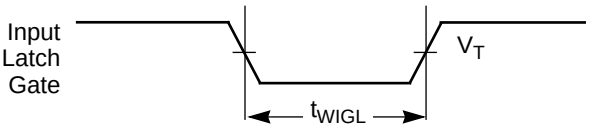
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



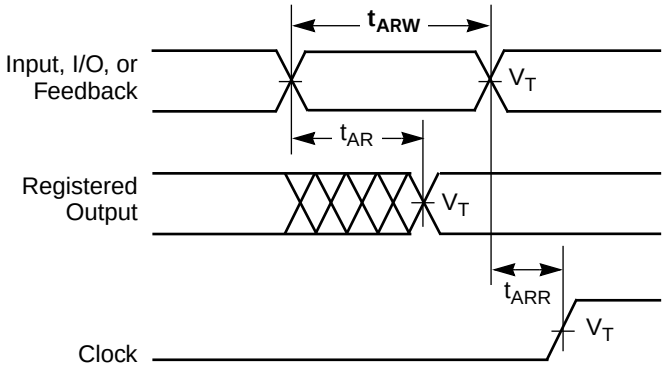
17466E-35

Input Register Clock Width



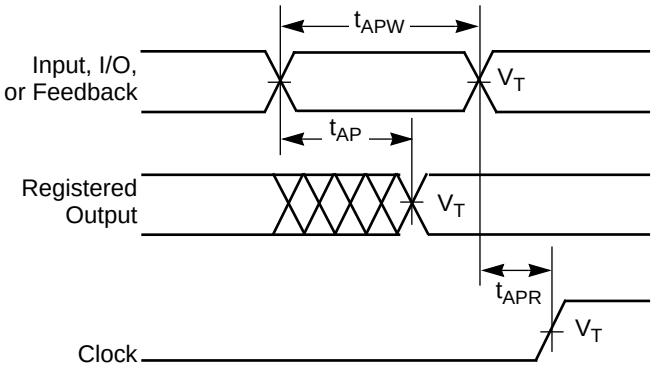
17466E-36

Input Latch Gate Width



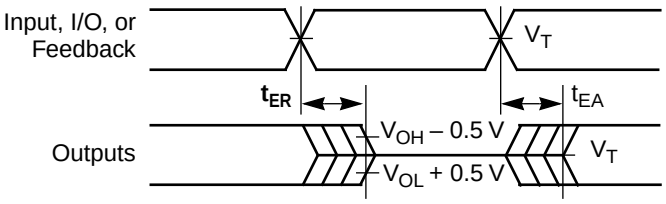
17466E-37

Asynchronous Reset



17466E-38

Asynchronous Preset



17466E-39

Output Disable/Enable

Notes:

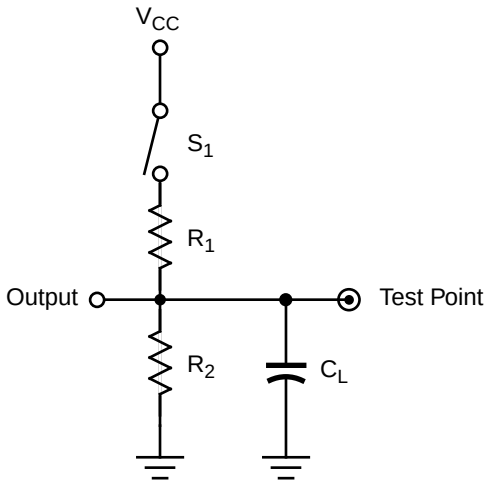
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



17466E-40

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	35 pF (30 pF)	300 Ω (1.6 KΩ)	390 Ω (1.6 KΩ)	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

Values in parentheses are for 3.3-V devices.

** Switching several outputs simultaneously should be avoided for accurate measurement.*

f_{MAX} PARAMETERS

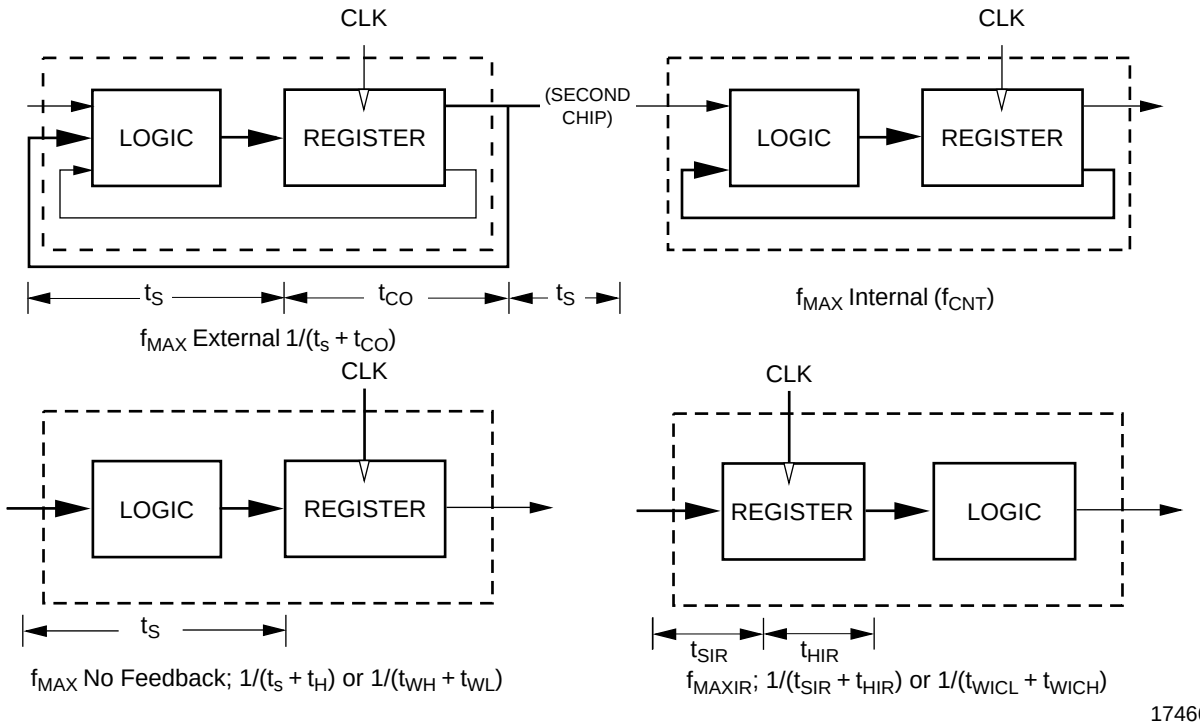
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "$f_{CNT.}$"

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

For devices with input registers, one additional f_{MAX} parameter is specified: f_{MAXIR}. Because this involves no feedback, it is calculated the same way as f_{MAX} no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that f_{MAXIR} is specified as $1/(t_{WICL} + t_{WICH})$. Note that if both input and output registers are used in the same path, the overall frequency will be limited by t_{ICS}. All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



17466E-41

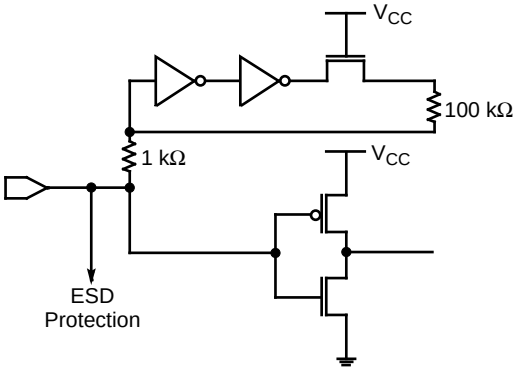
ENDURANCE CHARACTERISTICS

The MACH families are manufactured using Vantis' advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

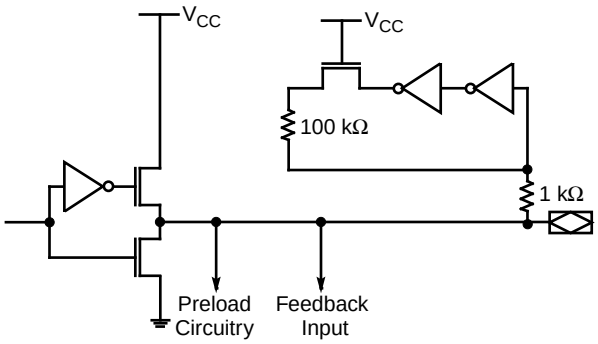
Endurance Characteristics

Parameter Symbol	Parameter Description		Units	Test Conditions
t_{DR}	Min Pattern Data Retention Time	10	Years	Max Storage Temperature
		20	Years	Max Operating Temperature
N	Max Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input



I/O

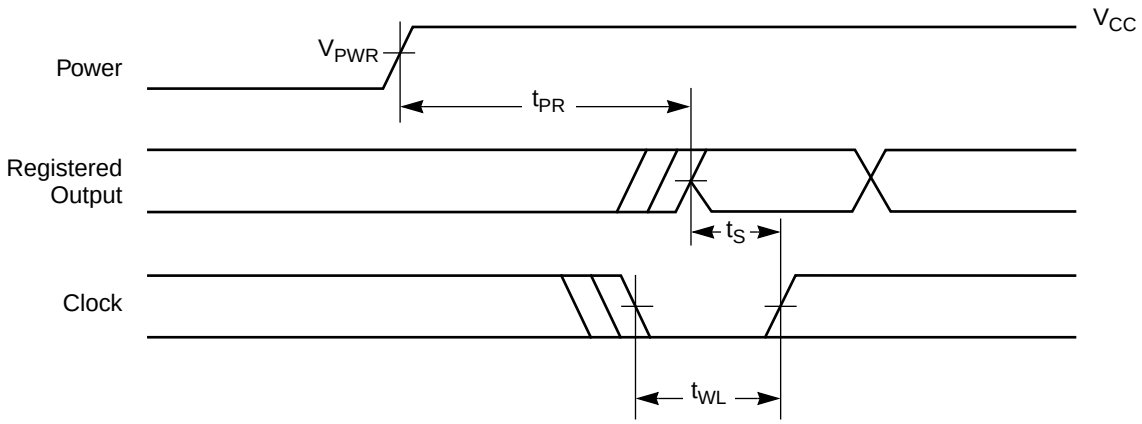
17466E-42

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



17466E-43

Power-Up Reset Waveform

V_{PWR} = 4 V for 5-V devices and 2.7 V for 3.3-V devices.

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the local Vantis sales office.

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Vantis Corporation P.O. Box 3755 920 DeGuigne Drive Sunnyvale, CA 94088 (408) 732-0555 or 1(888) 826-8472 (VANTIS2) http://www.vantis.com	MACHXL Software Vantis-ABEL Software Vantis-Synario Software
Aldec, Inc. 3 Sunset Way, Suite F Henderson, NV 89014 (702) 456-1222 or (800) 487-8743	ACTIVE-CAD
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234 or (800) 746-6223	PIC Designer Concept/Composer Synergy Leapfrog/Verilog-XL
Exemplar Logic, Inc. 815 Atlantic Avenue, Suite 105 Alameda, CA 94501 (510) 337-3700	Leonardo™ Galileo™
Logic Modeling 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (800) 346-6335	SmartModel® Library
Mentor Graphics Corp. 8005 S.W. Boeckman Rd. Wilsonville, OR 97070-7777 (800) 547-3000 or (503) 685-7000	Design Architect, PLDSynthesis™ II Autologic II Synthesizer, QuickSim Simulator, QuickHDL Simulator
MicroSim Corp. 20 Fairbanks Irvine, CA 92718 (714) 770-3022	MicroSim Design Lab PLogic, PLSyn
MINC Inc. 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (800) 755-FPGA or (719) 590-1155	PLDesigner-XL™ Software
Model Technology 8905 S.W. Nimbus Avenue, Suite 150 Beaverton, OR 97008 (503) 641-1340	V-System/VHDL
OrCAD, Inc. 9300 S.W. Nimbus Avenue Beaverton, OR 97008 (503) 671-9500 or (800) 671-9505	OrCAD Express
Synario® Design Automation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™ Synario™ Software

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Synopsys 700 E. Middlefield Rd. Mountain View, CA 94040 (415) 962-5000 or (800) 388-9125	FPGA or Design Compiler (Requires MINC PLDesigner-XL™) VSS Simulator
Synplicity, Inc. 624 East Evelyn Ave. Sunnyvale, CA 94086 (408) 617-6000	Synplify
Teradyne EDA 321 Harrison Ave. Boston, MA 02118 (800) 777-2432 or (617) 422-2793	MultiSIM Interactive Simulator LASAR
VeriBest, Inc. 6101 Lookout Road, Suite A Boulder, CO 80301 (800) 837-4237	VeriBest PLD
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 873-8439 or (508) 480-0881	Viewdraw, ViewPLD, Viewsynthesis Speedwave Simulator, ViewSim Simulator, VCS Simulator
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 881-8821	ATGEN™ Test Generation Software
iNt GmbH Busenstrasse 6 D-8033 Martinsried, Munich, Germany (87) 857-6667	PLDCheck 90

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APPROVED PROGRAMMERS (subject to change)

For more information on the products listed below, please consult the local Vantis sales office.

MANUFACTURER	PROGRAMMER CONFIGURATION
Advin Systems, Inc. 1050-L East Duane Ave. Sunnyvale, CA 940 86 (408) 243-7000 or (800) 627-2456 BBS (408) 737-9200 Fax (408) 736-2503	Pilot-U40 Pilot-U84 MVP
BP Microsystems 1000 N. Post Oak Rd., Suite 225 Houston, TX 77055-7237 (800) 225-2102 or (713) 688-4600 BBS (713) 688-9283 Fax (713) 688-0920	BP1200 BP1400 BP2100 BP2200
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 426-1045 or (206) 881-6444 BBS (206) 882-3211 Fax (206) 882-1043	UniSite™ Model 2900 Model 3900 AutoSite
Hi-Lo Systems 4F, No. 2, Sec. 5, Ming Shoh E. Road Taipei, Taiwan (886) 2-764-0215 Fax (886) 2-756-6403 or Tribal Microsystems / Hi-Lo Systems 44388 South Grimmer Blvd. Fremont, CA 94538 (510) 623-8859 BBS (510) 623-0430 Fax (510) 623-9925	ALL-07 FLEX-700
SMS GmbH Im Grund 15 88239 Wangen Germany (49) 7522-97280 Fax (49) 7522-972850 or SMS USA 544 Weddell Dr. Suite 12 Sunnyvale, CA 94089 (408) 542-0388	Sprint Expert Sprint Optima Multisite
Stag House Silver Court Watchmead, Welwyn Garden City Herfordshire UK AL7 1LT 44-1-707-332148 Fax 44-1-707-371503	Stag Quazar

MANUFACTURER	PROGRAMMER CONFIGURATION
System General 1603A South Main Street Milpitas, CA 95035 (408) 263-6667 BBS (408) 262-6438 Fax (408) 262-9220 or 3F, No. 1, Alley 8, Lane 45 Bao Shing Road, Shin Diau Taipei, Taiwan (886) 2-917-3005 Fax (886) 2-911-1283	Turpro-1 Turpro-1/FX Turpro-1/TX

APPROVED ADAPTER MANUFACTURERS

MANUFACTURER	PROGRAMMER CONFIGURATION
California Integration Coordinators, Inc. 656 Main Street Placerville, CA 95667 (916) 626-6168 Fax (916) 626-7740	MACH/PAL Programming Adapters
Emulation Technology, Inc. 2344 Walsh Ave., Bldg. F Santa Clara, CA 95051 (408) 982-0660 Fax (408) 982-0664	Adapt-A-Socket® Programming Adapters

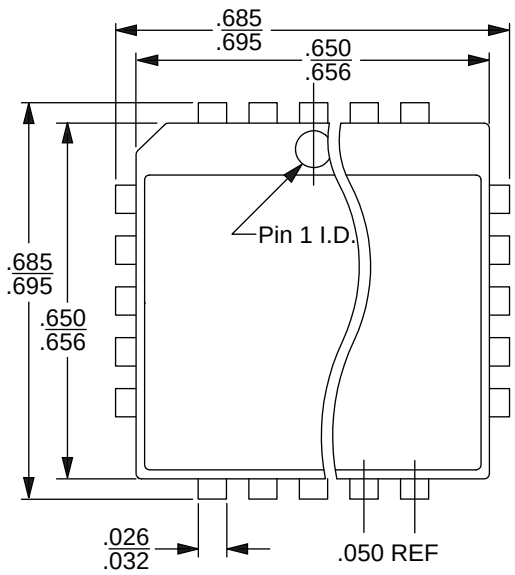
APPROVED ON-BOARD ISP PROGRAMMING TOOLS

MANUFACTURER	PROGRAMMER CONFIGURATION
Corelis, Inc. 12607 Hidden Creek Way, Suite H Cerritos, California 70703 (310) 926-6727	JTAGPROG™
Vantis Corporation P.O. Box 3755 920 DeGuigne Drive Sunnyvale, CA 94088 (408) 732-0555 or 1(888) 826-8472 (VANTIS2) http://www.vantis.com	MACHPRO®

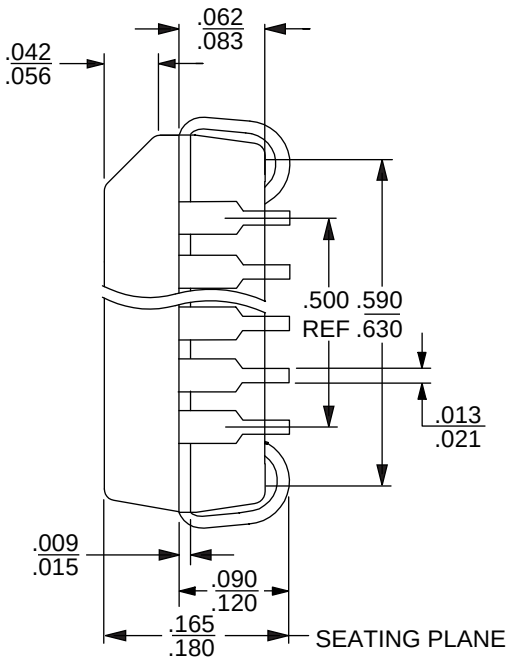
PHYSICAL DIMENSIONS

PL 044

44-Pin Plastic Leaded Chip Carrier (measured in inches)



TOP VIEW

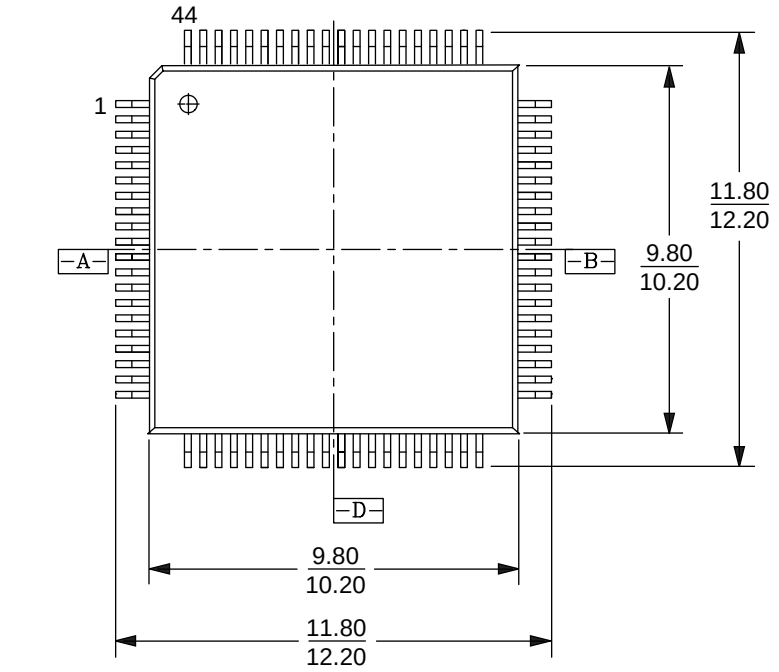


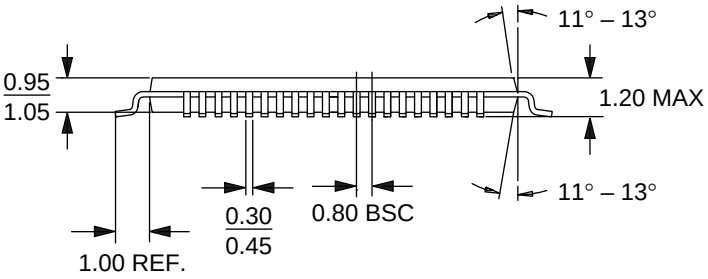
SIDE VIEW

16-038-SQ
PL 044
DA78
6-28-94 ae

PHYSICAL DIMENSIONS

PQT044
44-Pin Thin Quad Flat Pack (measured in inches)



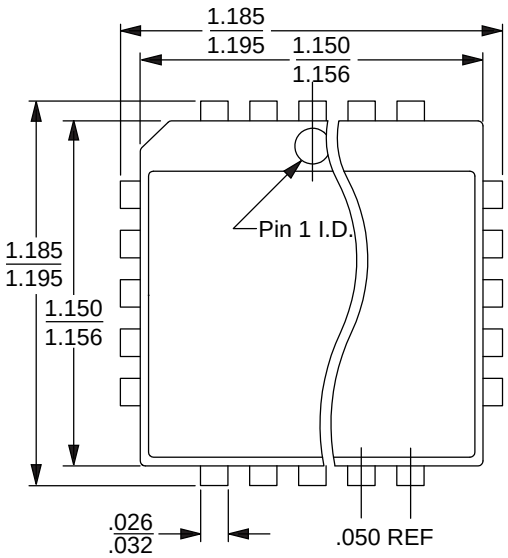


16-038-PQT-2
PQT 44
7-11-95 ae

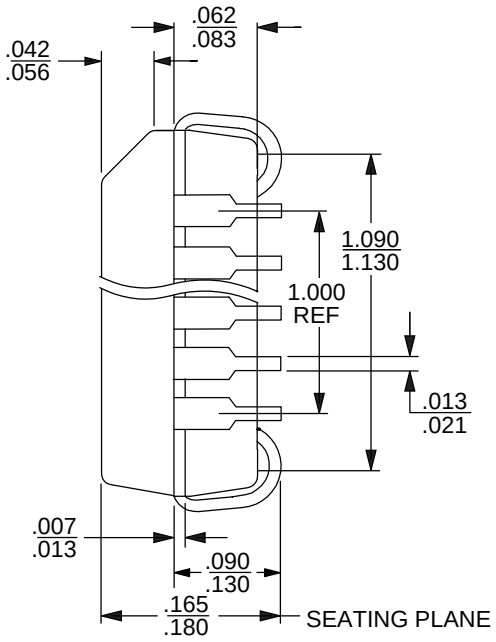
PHYSICAL DIMENSIONS

PL 084

84-Pin Plastic Leaded Chip Carrier (measured in inches)



TOP VIEW



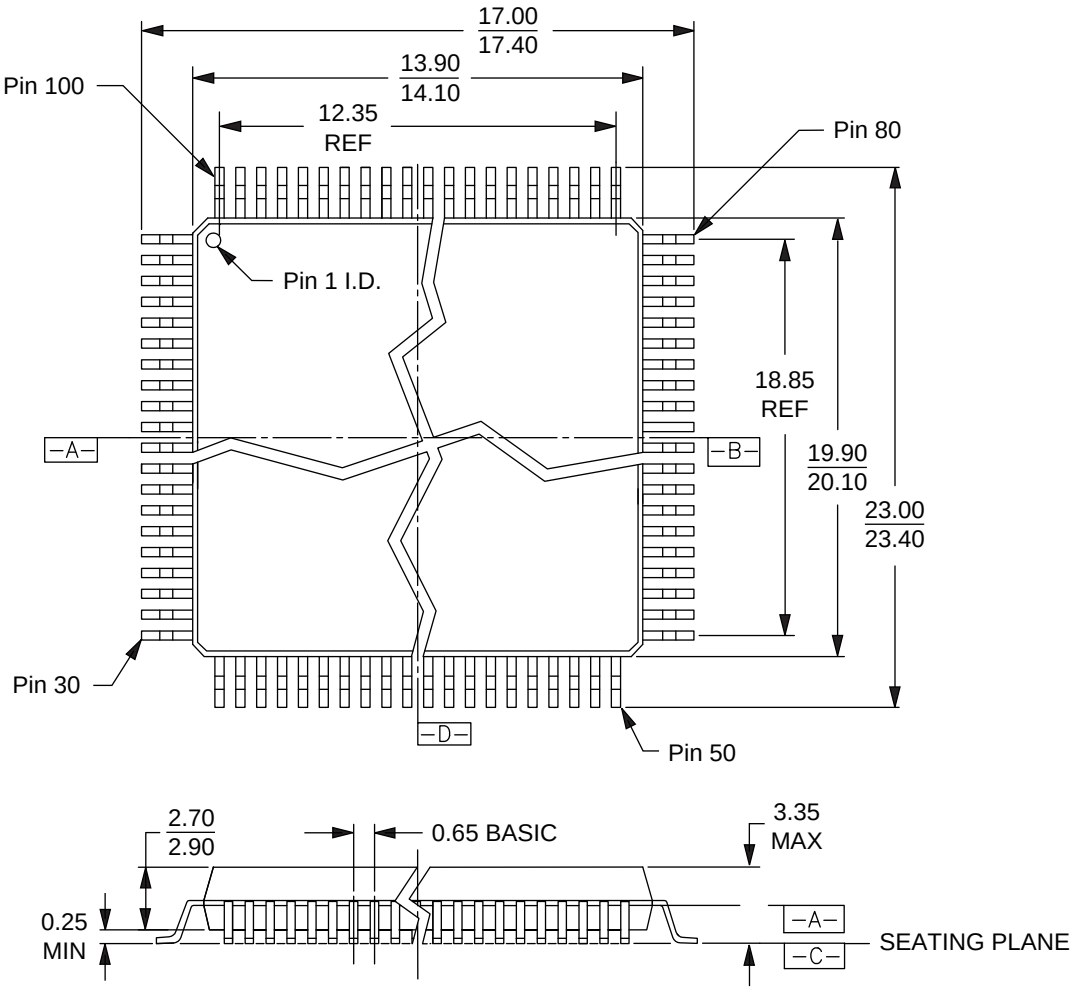
SIDE VIEW

16-038-SQ
PL 084
DF79
8-1-95 ae

PHYSICAL DIMENSIONS

PQR100

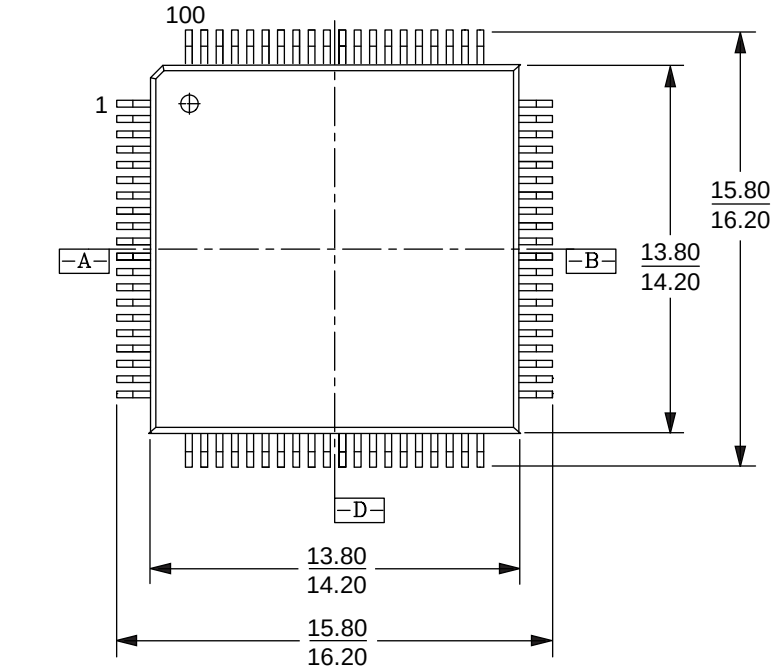
100-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)

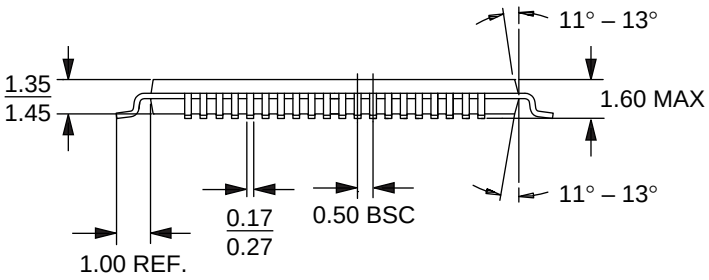


16-038-PQR-1_AH
PQR100
EC95
8-5-97 lv

PHYSICAL DIMENSIONS

PQL100
100-Pin Thin Quad Flat Pack



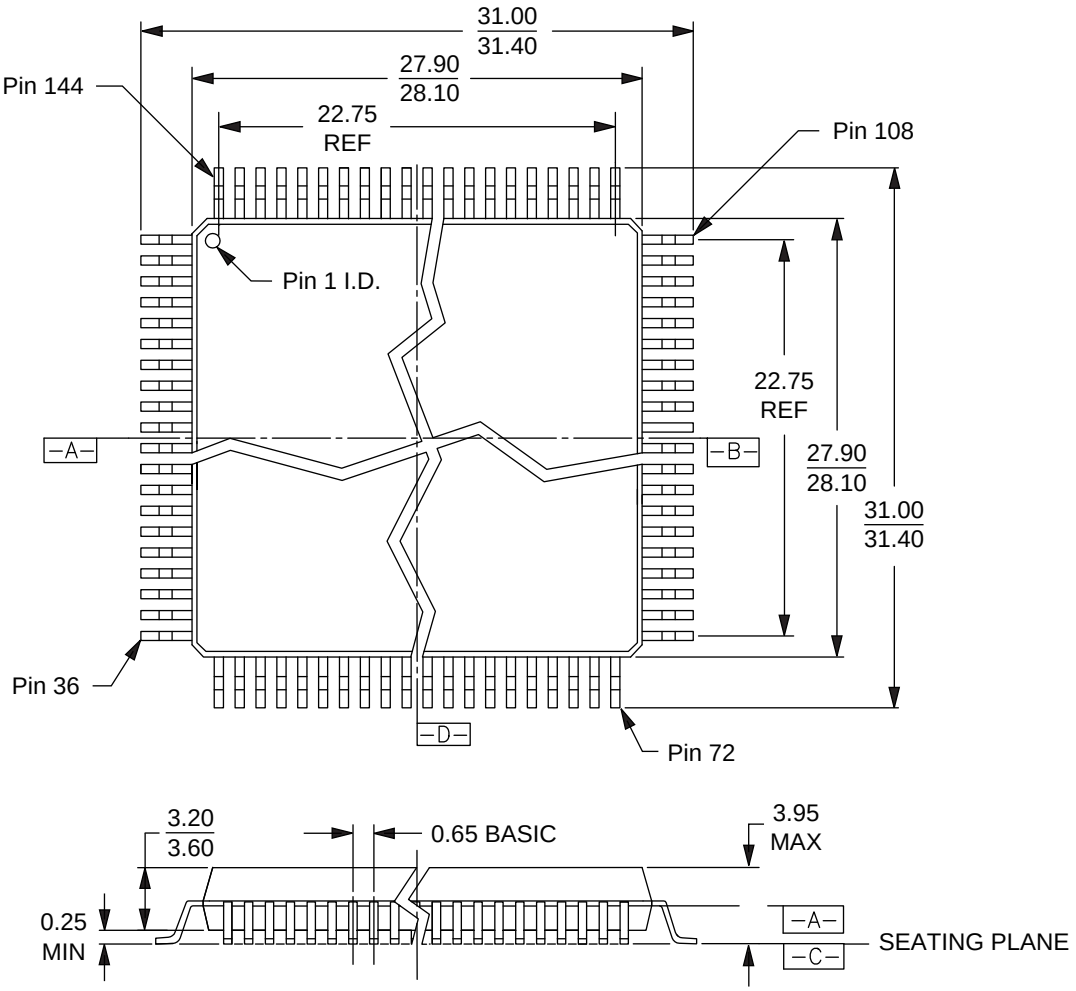


16-038-PQT-2_AI
PQL100
9.3.96 lv

PHYSICAL DIMENSIONS

PQR144

144-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)

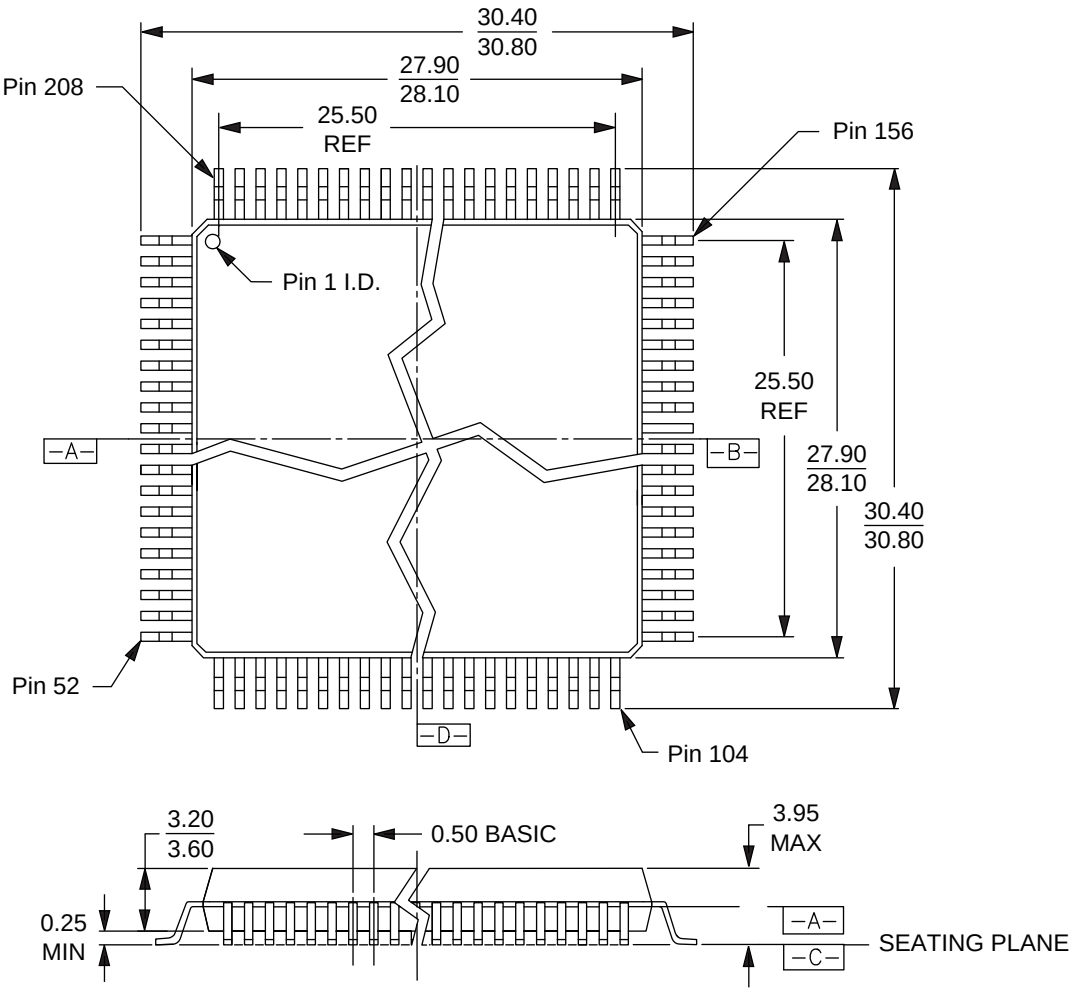


16-038-PQR-1_AH
PQR144
EC95
8-5-97 lv

PHYSICAL DIMENSIONS

PRH208

208-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)



16-038-PQR-1_AH
PRH208
EC95
8-13-97 lv