# MACH® 5 Family

## Fifth Generation MACH Architecture

## DISTINCTIVE CHARACTERISTICS

- **Fifth generation MACH architecture**
  - 100% routable
  - Pin-out retention
  - Four power/speed options per block for maximum performance and lowest power
  - Synchronous and asynchronous clocking, including dual-edge clocking
  - Asynchronous product- or sum-term reset
  - Functions of up to 32 product terms
  - Fixed, predictable delays
- **High speed**
  - 7.5 ns $t_{PD}$ Commercial, 10 ns $t_{PD}$ Industrial
  - 125 MHz $f_{CNT}$
- **High densities**
  - 128 to 512 macrocells
  - 16 to 64 output enables
  - Multiple density options for each package
- **System performance capabilities**
  - Both 5-V and JEDEC-compliant 3.3-V versions
  - In-system programmable
  - JTAG (IEEE 1149.1) boundary scan testing
  - PCI compliance (-7/-10/-12 speed grades)
  - Safe for mixed supply voltage system design
  - Bus-Friendly™ I/Os
  - Individual output slew rate control
  - Programmable security bit
- **Leading-edge process technology**
  - 0.35 and 0.5 micron ($L_{eff}$) processes
- **Supported by Vantis MACHXL® software**
  - Design entry ports to universal tools
  - Low-cost entry-level tool
  - Windows GUI interface
  - Auto device selection
  - Multiple device partitioning
- **Extensive software development support**
- **Third-party hardware programming support**



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## PRODUCT SELECTOR GUIDE

| Device | Macrocells | I/O Options | Speeds ($t_{PD}$) | Packages |
|---|---|---|---|---|
| M5-128<br>M5LV-128 | 128 | 68, 104, 120 | 7, 10, 12, 15 COM<br>10, 12, 15, 20 IND | PQFP, TQFP |
| M5-192<br>M5LV-192 | 192 | 68, 104, 120, 160 | 7, 10, 12, 15 COM<br>10, 12, 15, 20 IND | PQFP, TQFP |
| M5-256<br>M5LV-256 | 256 | 68, 104, 120, 160 | 7, 10, 12, 15 COM<br>10, 12, 15, 20 IND | PQFP, TQFP |
| M5-320<br>M5LV-320 | 320 | 120, 160, 184, 192 | 7, 10, 12, 15 COM<br>10, 12, 15, 20 IND | PQFP, BGA |
| M5-384<br>M5LV-384 | 384 | 120, 160, 184, 192 | 7, 10, 12, 15 COM<br>10, 12, 15, 20 IND | PQFP, BGA |
| M5-512<br>M5LV-512 | 512 | 120, 160, 184, 192, 256 | 7, 10, 12, 15 COM<br>10, 12, 15, 20 IND | PQFP, BGA |

## GENERAL DESCRIPTION

The MACH 5 family consists of a broad range of high-density, high-performance, and low-power complex programmable logic devices (CPLDs) with features such as in-system programmability, JTAG testability, and advanced clocking options. These fifth-generation MACH devices have advanced power management options which allow designers to incrementally reduce power. Both the 3.3-V and 5-V device versions are safe for mixed-voltage design, and the 7.5-, 10-, and 12-ns devices are compliant with the *PCI Local Bus Specification*. The MACH 5 family is manufactured in AMD's state-of-the-art ISO 9000 qualified fabrication facilities on 0.5- and 0.35- micron $L_{eff}$ EECMOS process technology.

All devices are available with pin-to-pin delays as fast as 7.5 ns and possess the density required for full system logic integration. The largest device, the M5-512, has 512 macrocells. The MACH 5 family's unique hierarchical architecture is ideal for PAL® device integration and a wide range of other applications including high-speed computing, low-power applications, communications, and embedded control.

Vantis offers software design support for MACH devices through its own development system and device fitters integrated into third-party CAE tools. Platform support extends across PCs, Sun and HP workstations under advanced operating systems such as Windows 3.1, Windows 95 and NT, SunOS and Solaris, and HPUX.

MACHXL software is a complete development system for the PC, supporting Vantis' MACH devices. It supports design entry with Boolean and behavioral syntax, state machine syntax and truth tables. Functional simulation and static timing analysis are also included in this easy-to-use system. This development system includes high-performance device fitters for all MACH devices.

The same fitter technology included in MACHXL software is seamlessly incorporated into third-party tools from leading CAE vendors such as Synario, Viewlogic, Mentor Graphics, Cadence and MINC. Interface kits and MACHXL configurations are also available to support design entry and verification with other leading vendors such as Synopsys, Exemplar, OrCAD, Synplicity and Model Technology. These MACHXL configurations and interfaces accept EDIF 2.0.0 netlists, generate JEDEC files for MACH devices, and create industry-standard SDF, VITAL-compliant VHDL and Verilog output files for design simulation.

Vantis offers in-system programming support for MACH devices through its MACHPRO® software enabling MACH device programmability through JTAG compliant ports and easy-to-use PC interface. Additionally, MACHPRO generated vectors work seamlessly with HP3070, GenRad and Teradyne testers to program MACH devices or test them for connectivity.

All MACH devices are supported by industry standard programmers available from a number of vendors. These programmer vendors include Advin Systems, BP Microsystems, Data I/O Corporation, Hi-Lo Systems, SMS GmbH, Stag House, and System General.

**Table 1. MACH Device Features**

| Feature | M5-128<br>M5LV-128 | M5-192<br>M5LV-192 | M5-256<br>M5LV-256 | M5-320<br>M5LV-320 | M5-384<br>M5LV-384 | M5-512<br>M5LV-512 |
|---|---|---|---|---|---|---|
| PLD Gates | 5000 | 7500 | 10000 | 12000 | 15000 | 20000 |
| Macrocells | 128 | 192 | 256 | 320 | 384 | 512 |
| Maximum I/O | 120 | 160 | 160 | 192 | 192 | 256 |
| Power (mA) | 35 | 45 | 55 | 70 | 75 | 100 |
| $t_{PD}$ (ns) | 7.5 | 7.5 | 7.5 | 7.5 | 7.5 | 7.5 |
| $t_{SS}$ (ns) | 4 | 4 | 4 | 4 | 4 | 4 |
| $t_{COS}$ (ns) | 6 | 6 | 6 | 6 | 6 | 6 |
| $f_{CNT}$ (MHz) | 125 | 125 | 125 | 125 | 125 | 125 |
| JTAG Compliant | Yes | Yes | Yes | Yes | Yes | Yes |
| PCI Compliant | -7/-10/-12 | -7/-10/-12 | -7/-10/-12 | -7/-10/-12 | -7/-10/-12 | -7/-10/-12 |

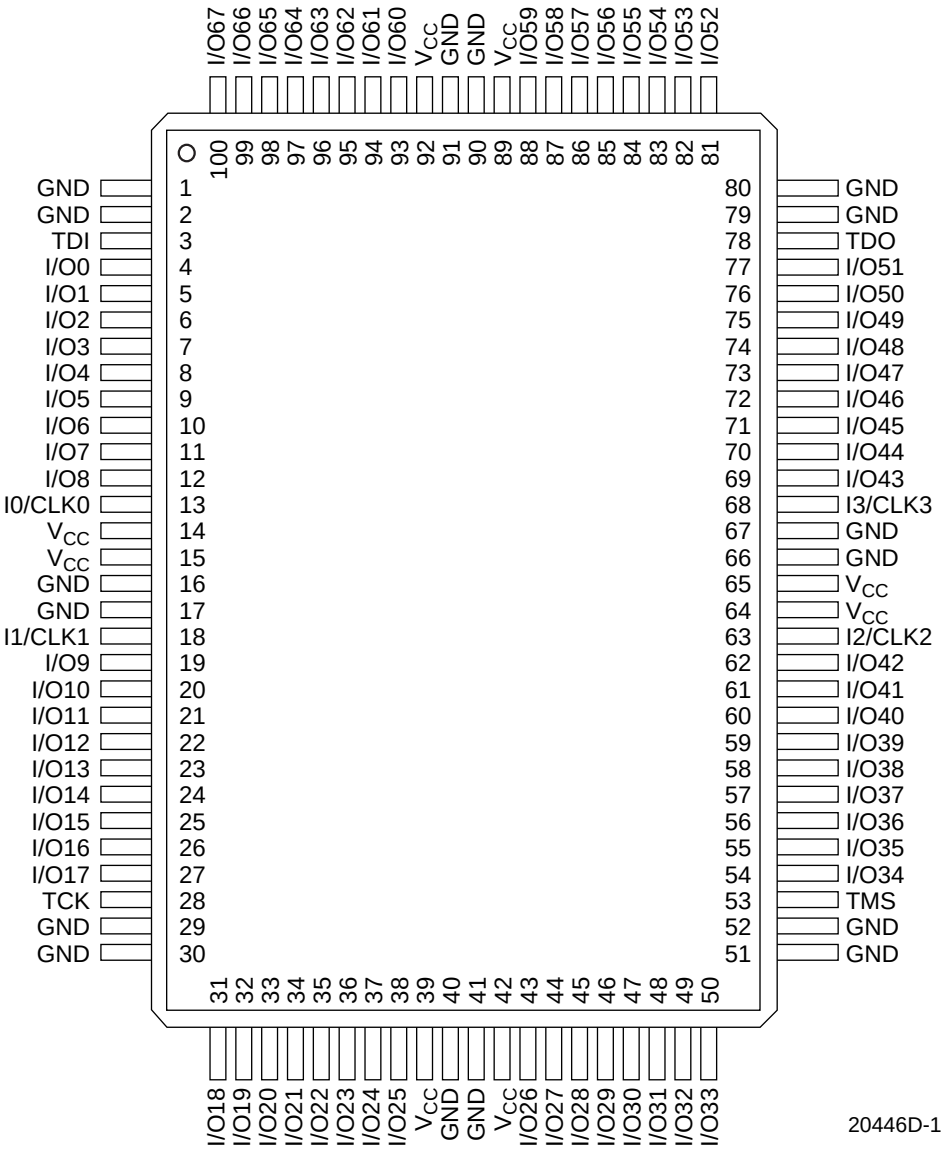
**Table 2. Package and Device Options**

| Package | M5-128<br>M5LV-128 | M5-192<br>M5LV-192 | M5-256<br>M5LV-256 | M5-320<br>M5LV-320 | M5-384<br>M5LV-384 | M5-512<br>M5LV-512 |
|---|---|---|---|---|---|---|
| 100 PQFP (68 I/O) | X | X | X | | | |
| 100 TQFP (68 I/O) | X | X | X | | | |
| 144 PQFP (104 I/O) | X | X | X | | | |
| 160 PQFP (120 I/O) | X | X | X | X | X | X |
| 208 PQFP (160 I/O) | | X | X | X | X | X |
| 240 PQFP (184 I/O) | | | | X | X | X |
| 256 BGA (192 I/O) | | | | X | X | X |
| 352 BGA (256 I/O) | | | | | | X |

# CONNECTION DIAGRAM

## Top View

**100-Pin PQFP**




20446D-1

M5-128/68, M5LV-128/68
M5-192/68, M5LV-192/68
M5-256/68, M5LV-256/68

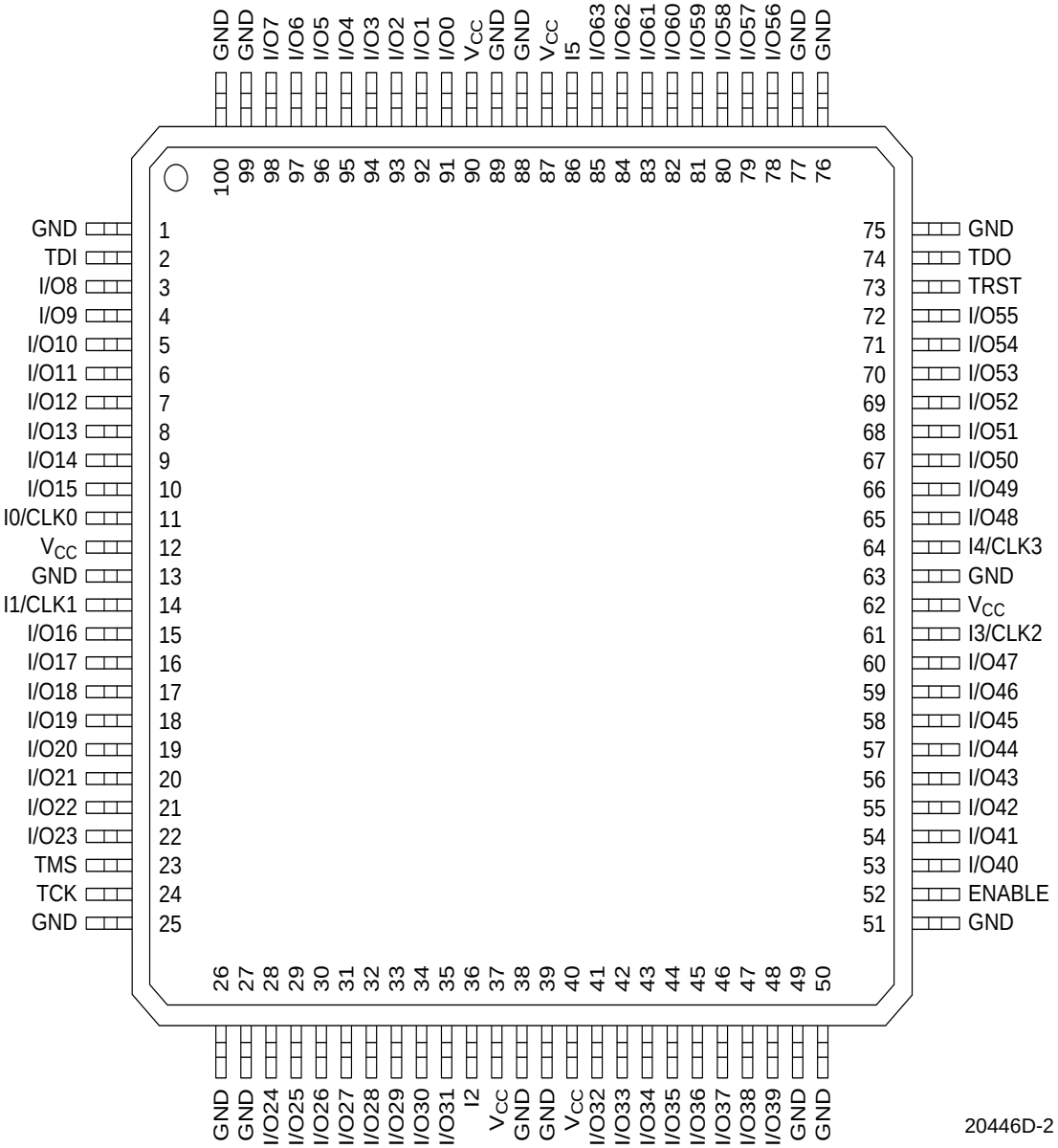
# PIN DESIGNATIONS

| | | | | | |
|---|---|---|---|---|---|
| CLK | = | Clock | TDI | = | Test Data In |
| GND | = | Ground | TCK | = | Test Clock |
| I | = | Input | TMS | = | Test Mode Select |
| I/O | = | Input/Output | TDO | = | Test Data Out |
| NC | = | No Connect | | | |
| $V_{CC}$ | = | Supply Voltage | | | |

# CONNECTION DIAGRAM

## Top View

**100-Pin TQFP**




20446D-2

M5-128/68, M5LV-128/68

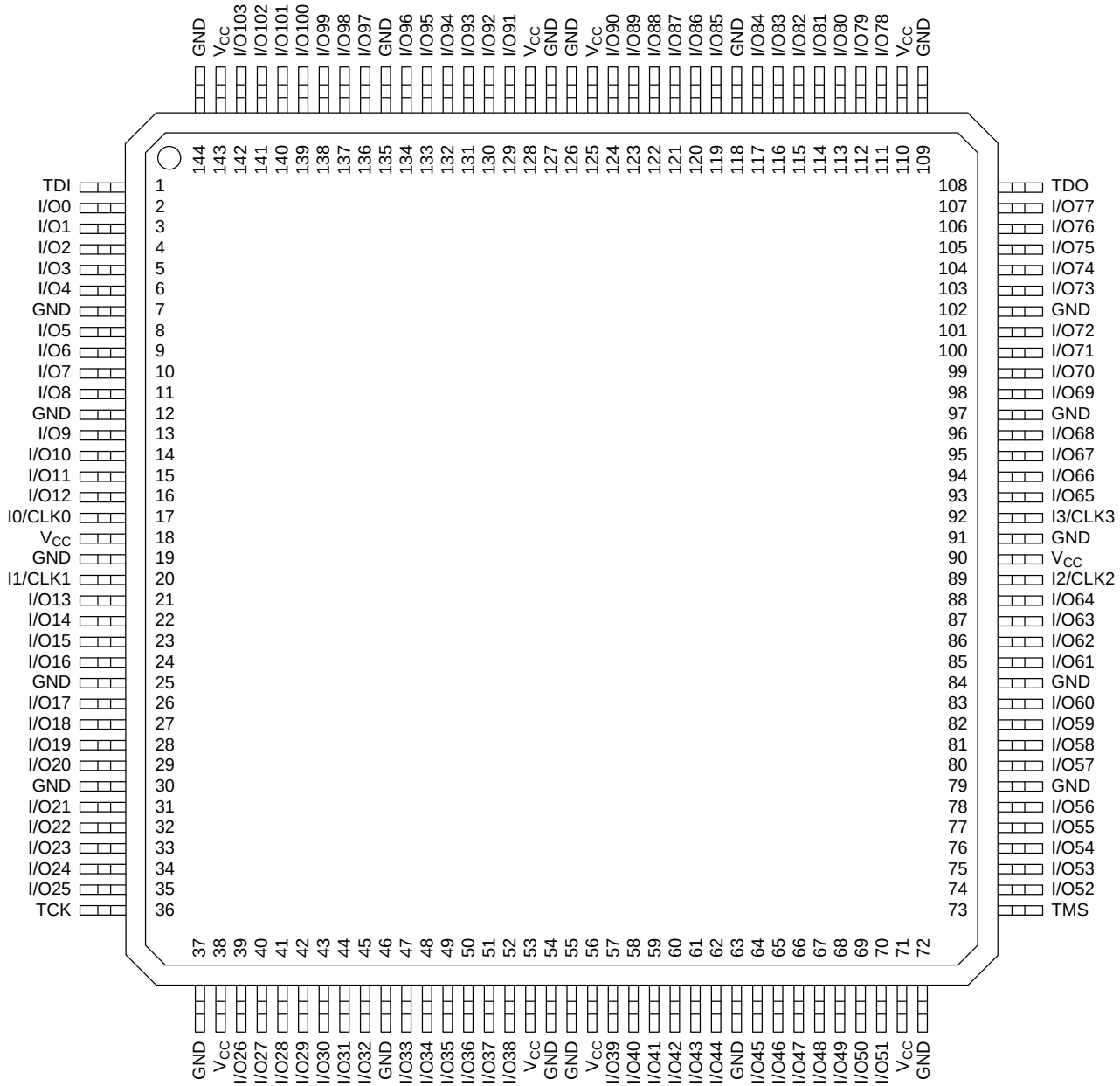
M5-192/68, M5LV-192/68

M5-256/68, M5LV-256/68

# CONNECTION DIAGRAM

## Top View

**144-Pin PQFP**




20446D-3

M5-128/104, M5LV-128/104

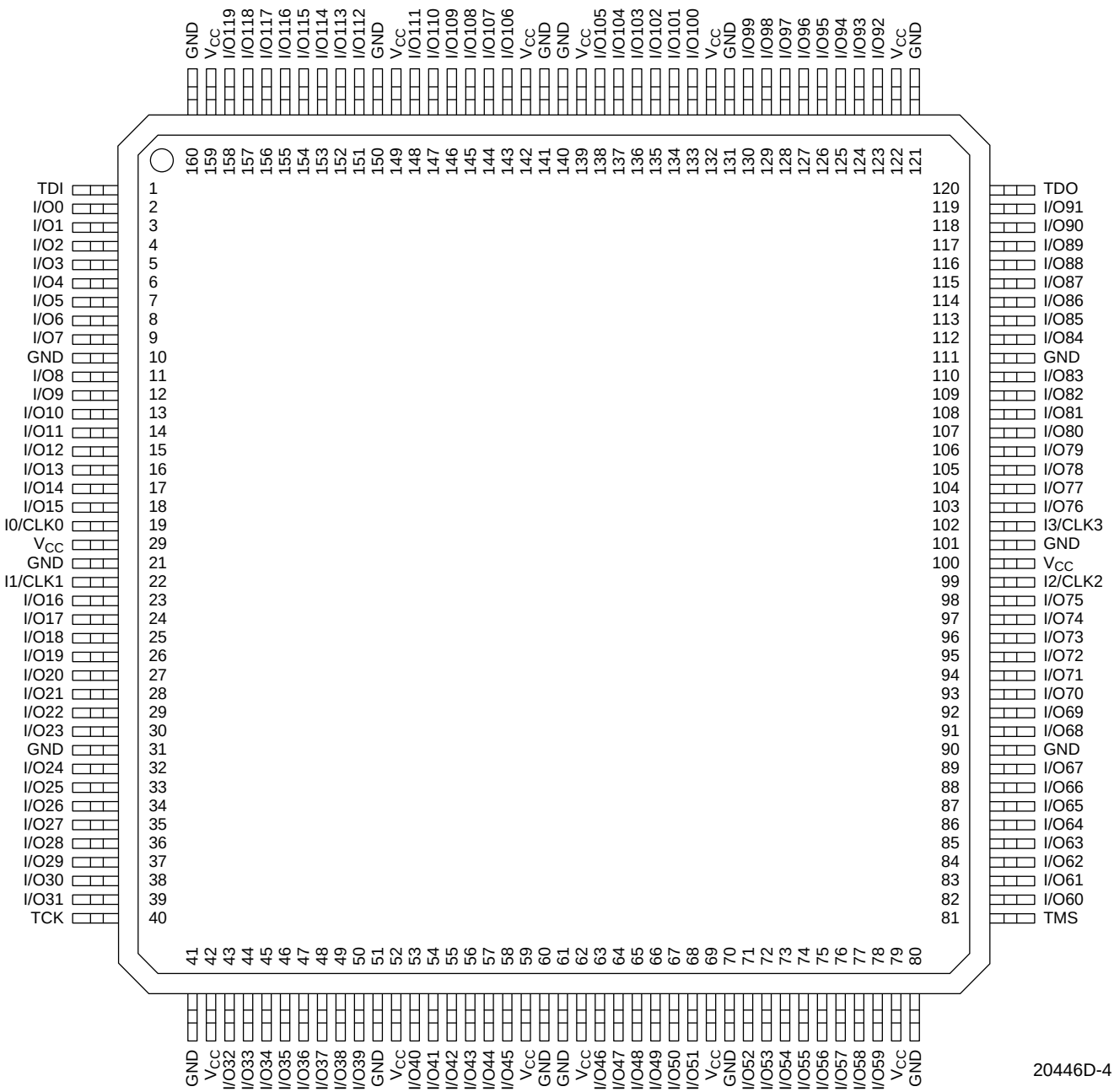
M5-192/104, M5LV-192/104

M5-256/104, M5LV-256/104

# CONNECTION DIAGRAM

## Top View

**160-Pin PQFP**




20446D-4

M5-128/120, M5LV-128/120

M5-192/120, M5LV-192/120

M5-256/120, M5LV-256/120

M5-320/120, M5LV-320/120

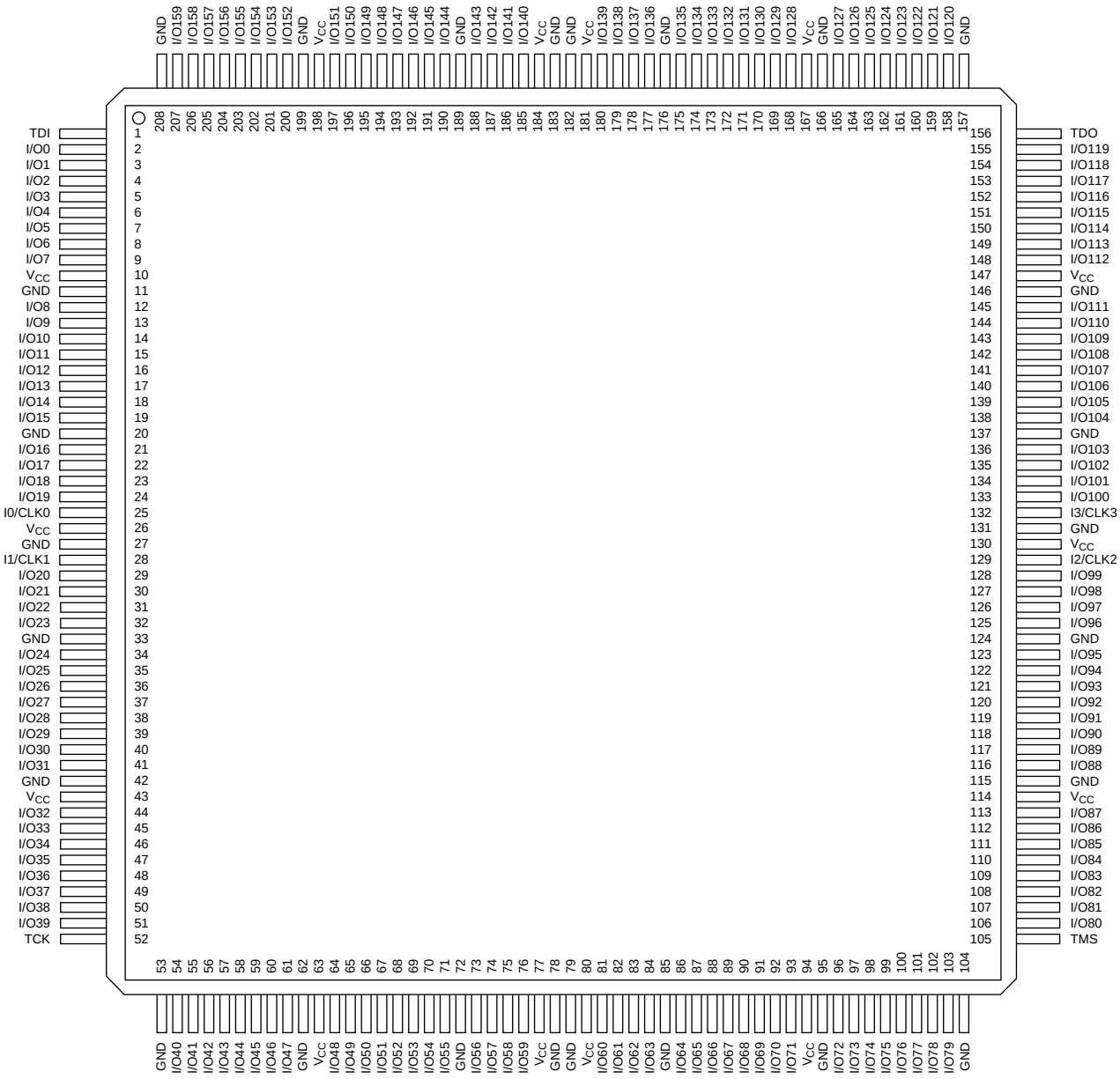
M5-384/120, M5LV-384/120

M5-512/120, M5LV-512/120

# CONNECTION DIAGRAM

## Top View

**208-Pin PQFP**




20446D-5

M5-192/160, M5LV-192/160

M5-256/160, M5LV-256/160

M5-320/160, M5LV-320/160

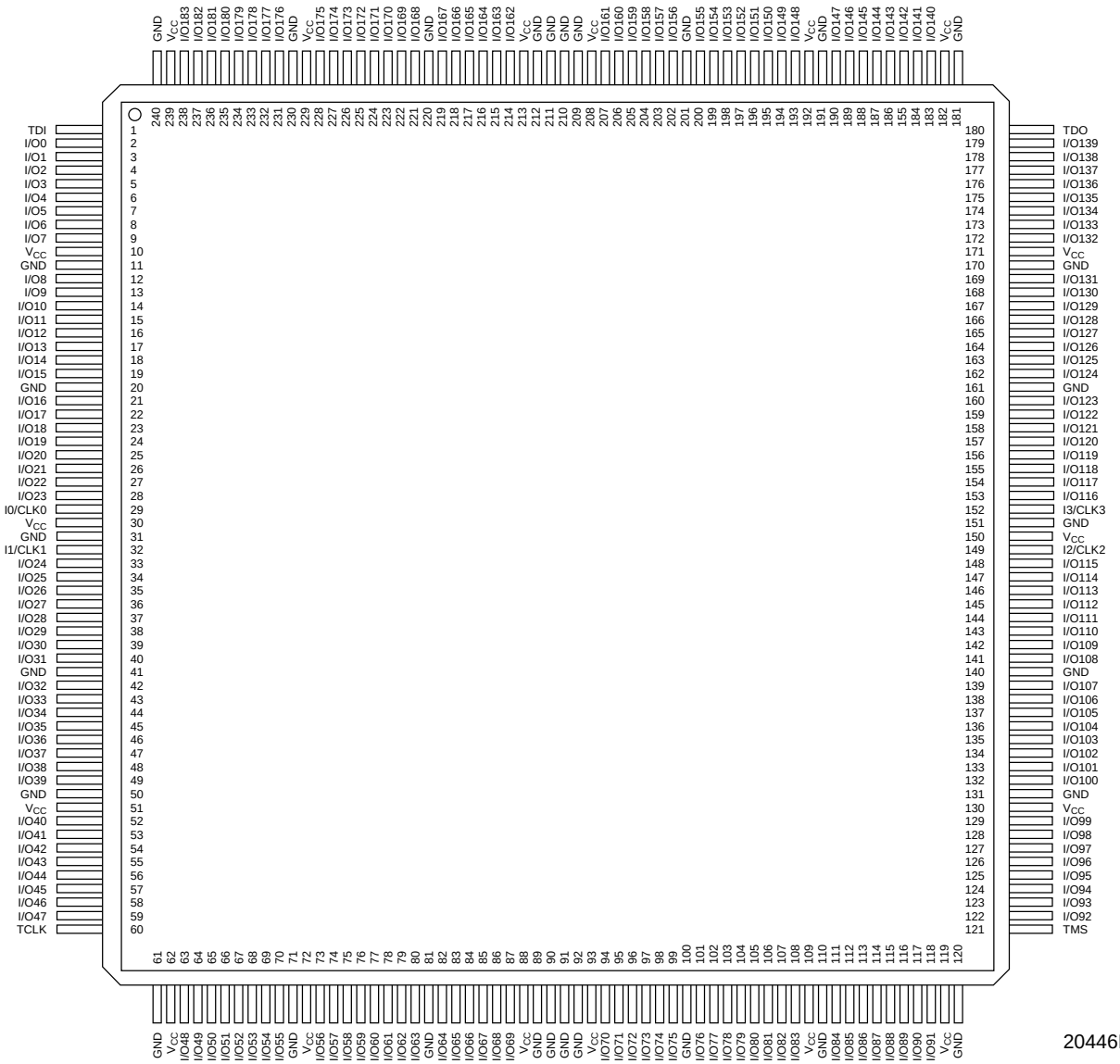
M5-384/160, M5LV-384/160

M5-512/160, M5LV-512/160

# CONNECTION DIAGRAM

## Top View

**240-Pin PQFP**




20446D-6

M5-320/184, M5LV-320/184

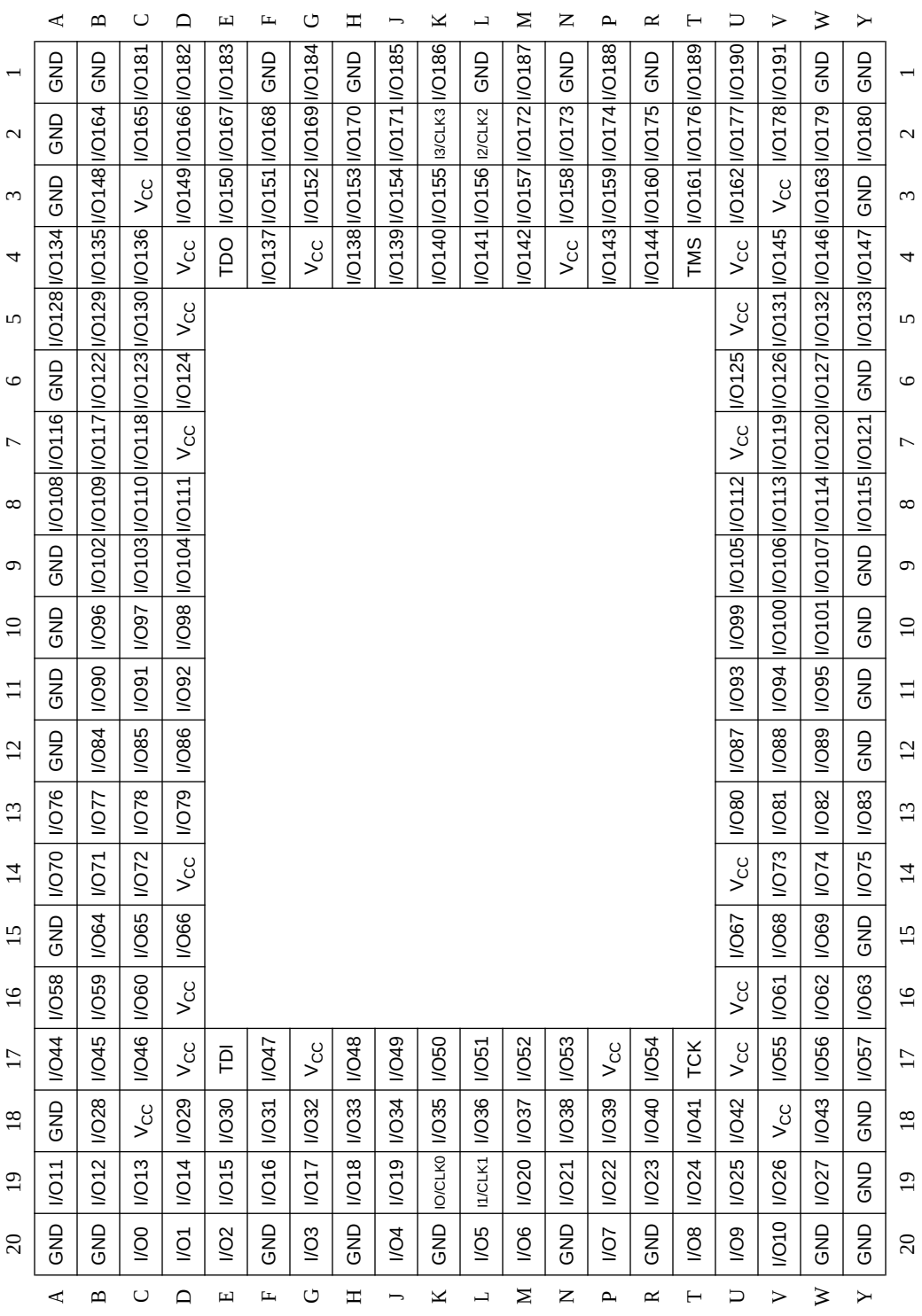
M5-384/184, M5LV-384/184

M5-512/184, M5LV-512/184

# CONNECTION DIAGRAM

## Bottom View

**256-Pin BGA**



| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | V | W | Y | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | GND | GND | I/O181 | I/O182 | I/O183 | GND | I/O184 | GND | I/O185 | I/O186 | GND | I/O187 | GND | I/O188 | GND | I/O189 | I/O190 | I/O191 | GND | GND | 1 |
| 2 | GND | I/O164 | I/O165 | I/O166 | I/O167 | I/O168 | I/O169 | I/O170 | I/O171 | I/O172 | I2/CLK2 | I/O173 | I/O174 | I/O175 | I/O176 | I/O177 | I/O178 | I/O179 | I/O180 | 2 | |
| 3 | GND | I/O148 | $V_{CC}$ | I/O149 | I/O150 | I/O151 | I/O152 | I/O153 | I/O154 | I/O155 | I3/CLK3 | I/O156 | I/O157 | I/O158 | I/O159 | I/O160 | I/O161 | $V_{CC}$ | I/O162 | I/O163 | GND | 3 |
| 4 | I/O134 | I/O135 | I/O136 | $V_{CC}$ | TDO | I/O137 | $V_{CC}$ | I/O138 | I/O139 | I/O140 | I/O141 | I/O142 | $V_{CC}$ | I/O143 | I/O144 | TMS | $V_{CC}$ | I/O145 | I/O146 | I/O147 | 4 | |
| 5 | I/O128 | I/O129 | I/O130 | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | I/O131 | I/O132 | I/O133 | 5 | |
| 6 | GND | I/O122 | I/O123 | I/O124 | | | | | | | | | | | | | I/O125 | I/O126 | I/O127 | GND | 6 | |
| 7 | I/O116 | I/O117 | I/O118 | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | I/O119 | I/O120 | I/O121 | 7 | |
| 8 | I/O108 | I/O109 | I/O110 | I/O111 | | | | | | | | | | | | | I/O112 | I/O113 | I/O114 | I/O115 | 8 | |
| 9 | GND | I/O102 | I/O103 | I/O104 | | | | | | | | | | | | | I/O105 | I/O106 | I/O107 | GND | 9 | |
| 10 | GND | I/O96 | I/O97 | I/O98 | | | | | | | | | | | | | I/O99 | I/O100 | I/O101 | GND | 10 | |
| 11 | GND | I/O90 | I/O91 | I/O92 | | | | | | | | | | | | | I/O93 | I/O94 | I/O95 | GND | 11 | |
| 12 | GND | I/O84 | I/O85 | I/O86 | | | | | | | | | | | | | I/O87 | I/O88 | I/O89 | GND | 12 | |
| 13 | I/O76 | I/O77 | I/O78 | I/O79 | | | | | | | | | | | | | I/O80 | I/O81 | I/O82 | I/O83 | 13 | |
| 14 | I/O70 | I/O71 | I/O72 | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | I/O73 | I/O74 | I/O75 | 14 | |
| 15 | GND | I/O64 | I/O65 | I/O66 | | | | | | | | | | | | | I/O67 | I/O68 | I/O69 | GND | 15 | |
| 16 | I/O58 | I/O59 | I/O60 | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | I/O61 | I/O62 | I/O63 | 16 | |
| 17 | I/O44 | I/O45 | I/O46 | $V_{CC}$ | TDI | I/O47 | $V_{CC}$ | I/O48 | I/O49 | I/O50 | I/O51 | I/O52 | I/O53 | $V_{CC}$ | I/O54 | TCK | $V_{CC}$ | I/O55 | I/O56 | I/O57 | 17 | |
| 18 | GND | I/O28 | $V_{CC}$ | I/O29 | I/O30 | I/O31 | I/O32 | I/O33 | I/O34 | I/O35 | I/O36 | I/O37 | I/O38 | I/O39 | I/O40 | I/O41 | I/O42 | $V_{CC}$ | I/O43 | GND | 18 | |
| 19 | I/O11 | I/O12 | I/O13 | I/O14 | I/O15 | I/O16 | I/O17 | I/O18 | I/O19 | I/O/CLK0 | I1/CLK1 | I/O20 | I/O21 | I/O22 | I/O23 | I/O24 | I/O25 | I/O26 | I/O27 | GND | 19 | |
| 20 | GND | GND | I/O0 | I/O1 | I/O2 | GND | I/O3 | GND | I/O4 | GND | I/O5 | I/O6 | GND | I/O7 | GND | I/O8 | I/O9 | I/O10 | GND | GND | 20 | |

20446D-7

M5-320/192, M5LV-320/192

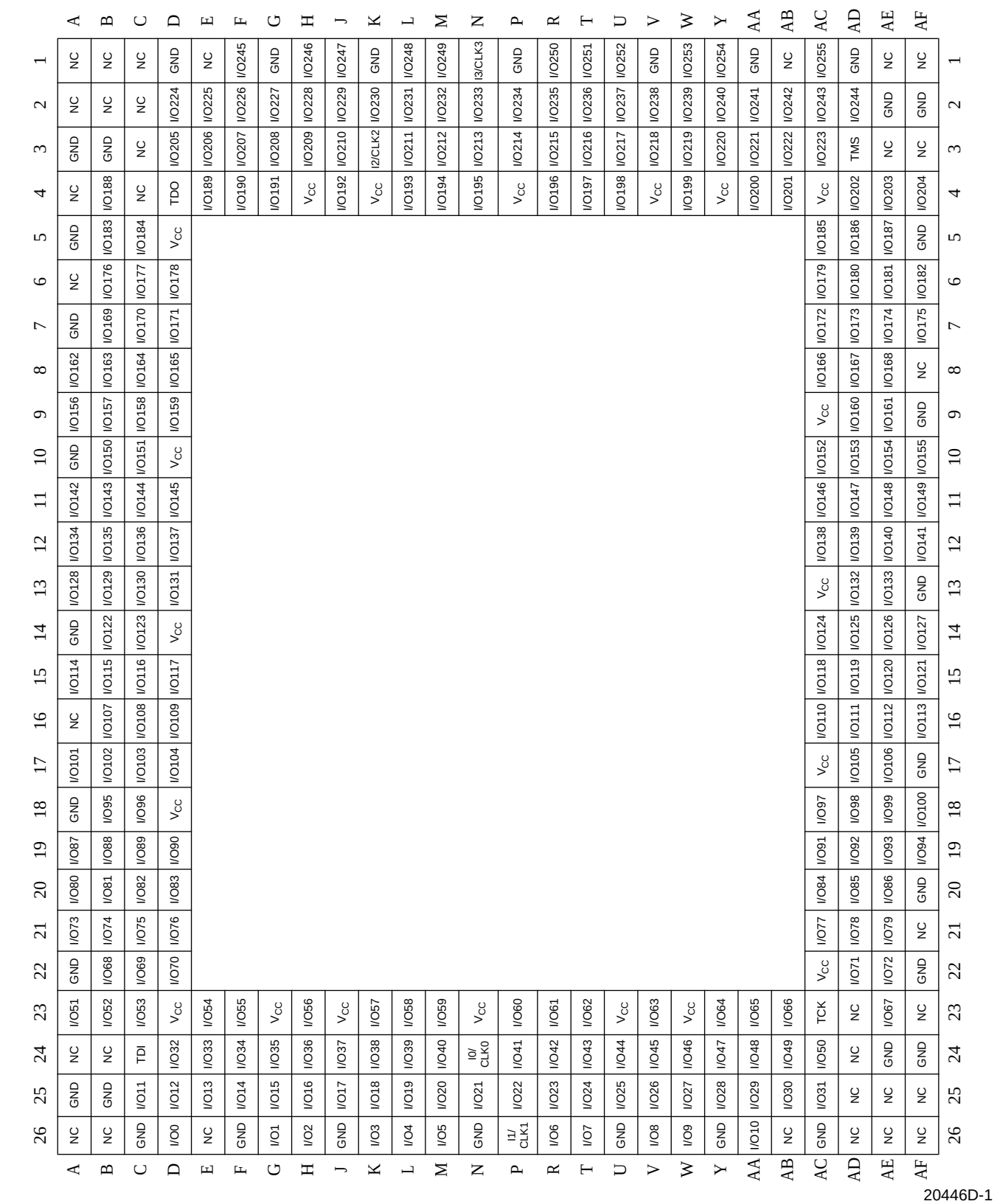
M5-384/192, M5LV-384/192

M5-512/192, M5LV-512/192

# CONNECTION DIAGRAM

## Bottom View

**352-Pin BGA**




20446D-1

M5-512/256, M5LV-512/256

# ORDERING INFORMATION

## MACH 5 COM -7.5, -10, -12, -15

Vantis standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

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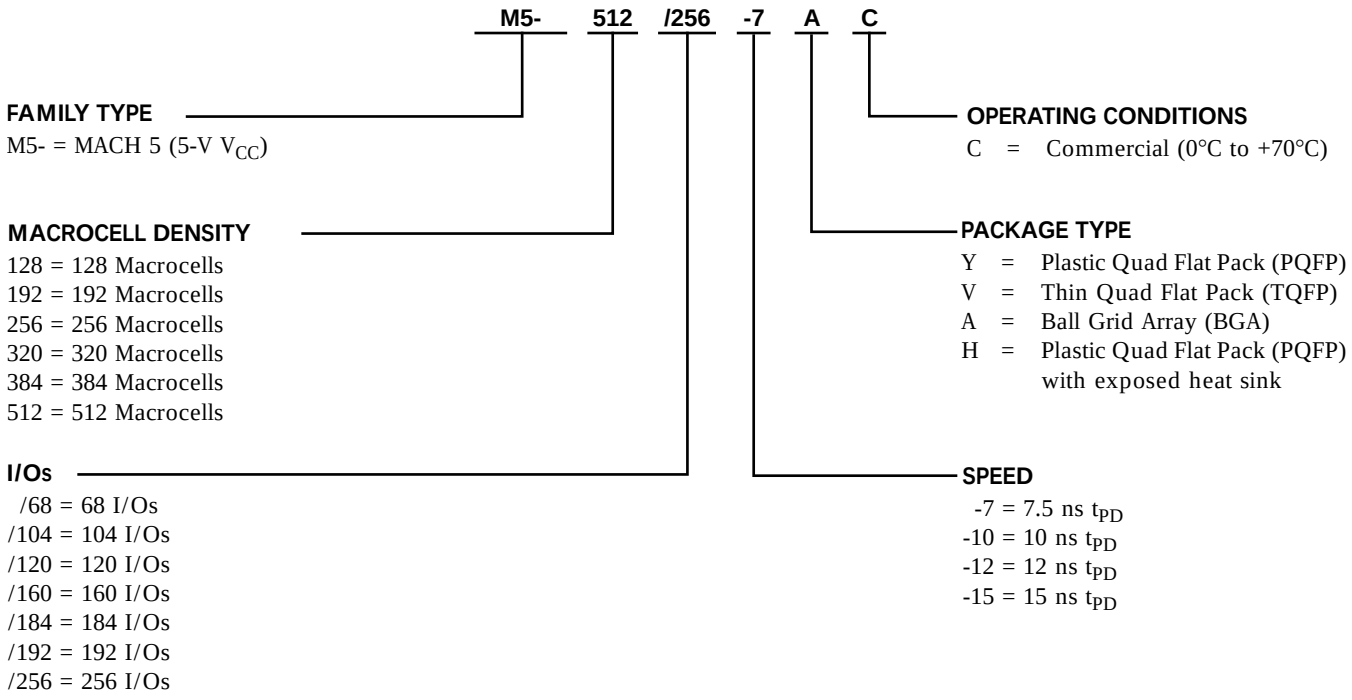


| Valid Combinations | | |
|---|---|---|
| M5-128/68 | -7, -10, -12, -15 | YC, VC |
| M5-128/104 | | YC |
| M5-128/120 | | YC |
| M5-192/68 | | YC, VC |
| M5-192/104 | | YC |
| M5-192/120 | | YC |
| M5-192/160 | | YC |
| M5-256/68 | | YC, VC |
| M5-256/104 | | YC |
| M5-256/120 | | YC |
| M5-256/160 | | YC |

**Device Marking**

Actual device marking differs from the ordering part number (OPN). “MACH 5” is marked on a device wherever “M5-” is used in the OPN.

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| Valid Combinations | | |
|---|---|---|
| M5-320/120 | -7, -10, -12, -15 | HC |
| M5-320/160 | | HC |
| M5-320/184 | | HC |
| M5-320/192 | | AC |
| M5-384/120 | | HC |
| M5-384/160 | | HC |
| M5-384/184 | | HC |
| M5-384/192 | | AC |
| M5-512/120 | | HC |
| M5-512/160 | | HC |
| M5-512/184 | | HC |
| M5-512/192 | | AC |
| M5-512/256 | | AC |

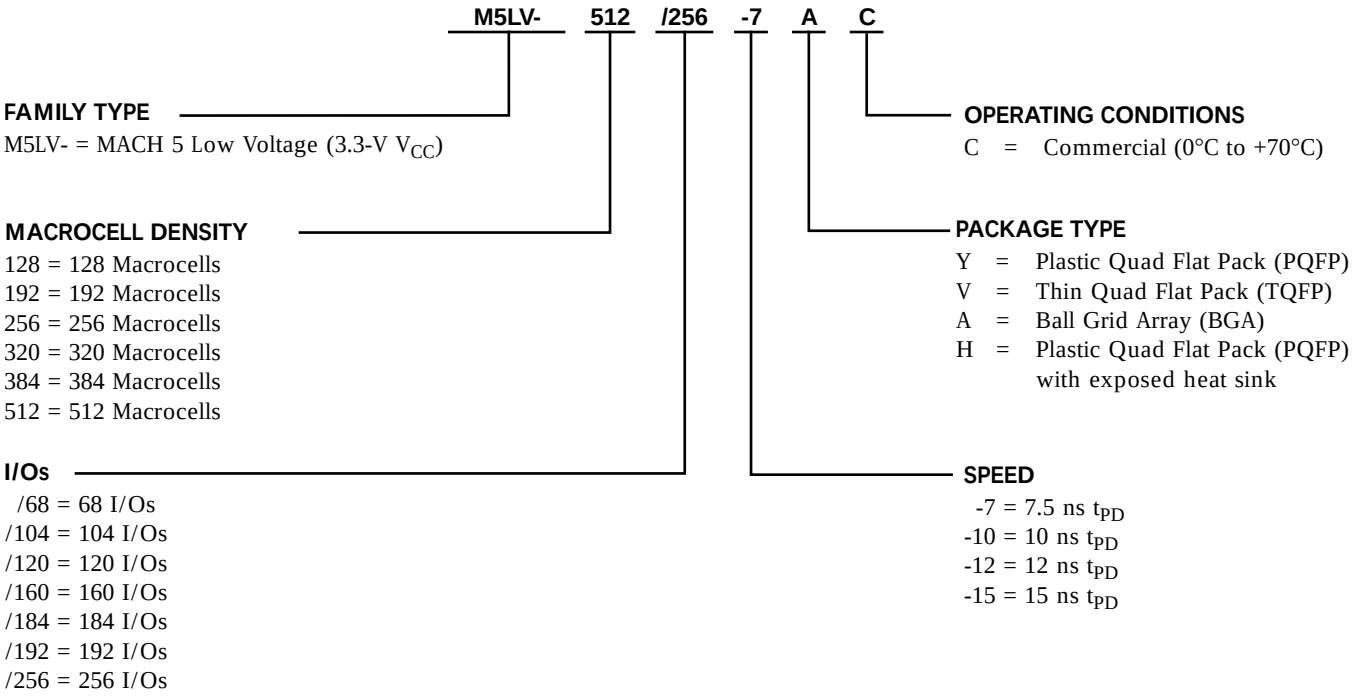
**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

# ORDERING INFORMATION

## MACH 5 LV COM -7.5, -10, -12, -15

Vantis standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.




| Valid Combinations | | |
|---|---|---|
| M5LV-128/68 | -7, -10, -12, -15 | YC, VC |
| M5LV-128/104 | | YC |
| M5LV-128/120 | | YC |
| M5LV-192/68 | | YC, VC |
| M5LV-192/104 | | YC |
| M5LV-192/120 | | YC |
| M5LV-192/160 | | YC |
| M5LV-256/68 | | YC, VC |
| M5LV-256/104 | | YC |
| M5LV-256/120 | | YC |
| M5LV-256/160 | | YC |

### Device Marking

Actual device marking differs from the ordering part number (OPN). “MACH 5” is marked on a device wherever “M5-” is used in the OPN.

| Valid Combinations | | |
|---|---|---|
| M5LV-320/120 | -7, -10, -12, -15 | HC |
| M5LV-320/160 | | HC |
| M5LV-320/184 | | HC |
| M5LV-320/192 | | AC |
| M5LV-384/120 | | HC |
| M5LV-384/160 | | HC |
| M5LV-384/184 | | AC |
| M5LV-384/192 | | HC |
| M5LV-512/120 | | HC |
| M5LV-512/160 | | HC |
| M5LV-512/184 | | HC |
| M5LV-512/192 | | AC |
| M5LV-512/256 | | AC |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

# ORDERING INFORMATION

## MACH 5 IND -10, -12, -15, -20

Vantis standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

**M5- 512 /256 -10 A I**

**FAMILY TYPE**
M5- = MACH 5 (5-V $V_{CC}$)

**MACROCELL DENSITY**
128 = 128 Macrocells
192 = 192 Macrocells
256 = 256 Macrocells
320 = 320 Macrocells
384 = 384 Macrocells
512 = 512 Macrocells

**I/Os**
/68 = 68 I/Os
/104 = 104 I/Os
/120 = 120 I/Os
/160 = 160 I/Os
/184 = 184 I/Os
/192 = 192 I/Os
/256 = 256 I/Os

**SPEED**
-10 = 10 ns $t_{PD}$
-12 = 12 ns $t_{PD}$
-15 = 15 ns $t_{PD}$
-20 = 20 ns $t_{PD}$

**PACKAGE TYPE**
Y = Plastic Quad Flat Pack (PQFP)
V = Thin Quad Flat Pack (TQFP)
A = Ball Grid Array (BGA)
H = Plastic Quad Flat Pack (PQFP) with exposed heat sink

**OPERATING CONDITIONS**
I = Industrial (–40°C to +85°C)

| Valid Combinations | | |
|---|---|---|
| M5-128/68 | -10, -12, -15, -20 | YI, VI |
| M5-128/104 | | YI |
| M5-128/120 | | YI |
| M5-192/68 | | YI, VI |
| M5-192/104 | | YI |
| M5-192/120 | | YI |
| M5-192/160 | | YI |
| M5-256/68 | | YI, VI |
| M5-256/104 | | YI |
| M5-256/120 | | YI |
| M5-256/160 | | YI |

**Device Marking**

Actual device marking differs from the ordering part number (OPN). “MACH 5” is marked on a device wherever “M5-” is used in the OPN.

| Valid Combinations | | |
|---|---|---|
| M5-320/120 | -10, -12, -15, -20 | HI |
| M5-320/160 | | HI |
| M5-320/184 | | HI |
| M5-320/192 | | AI |
| M5-384/120 | | HI |
| M5-384/160 | | HI |
| M5-384/184 | | HI |
| M5-384/192 | | AI |
| M5-512/120 | | HI |
| M5-512/160 | | HI |
| M5-512/184 | | HI |
| M5-512/192 | | AI |
| M5-512/256 | | AI |

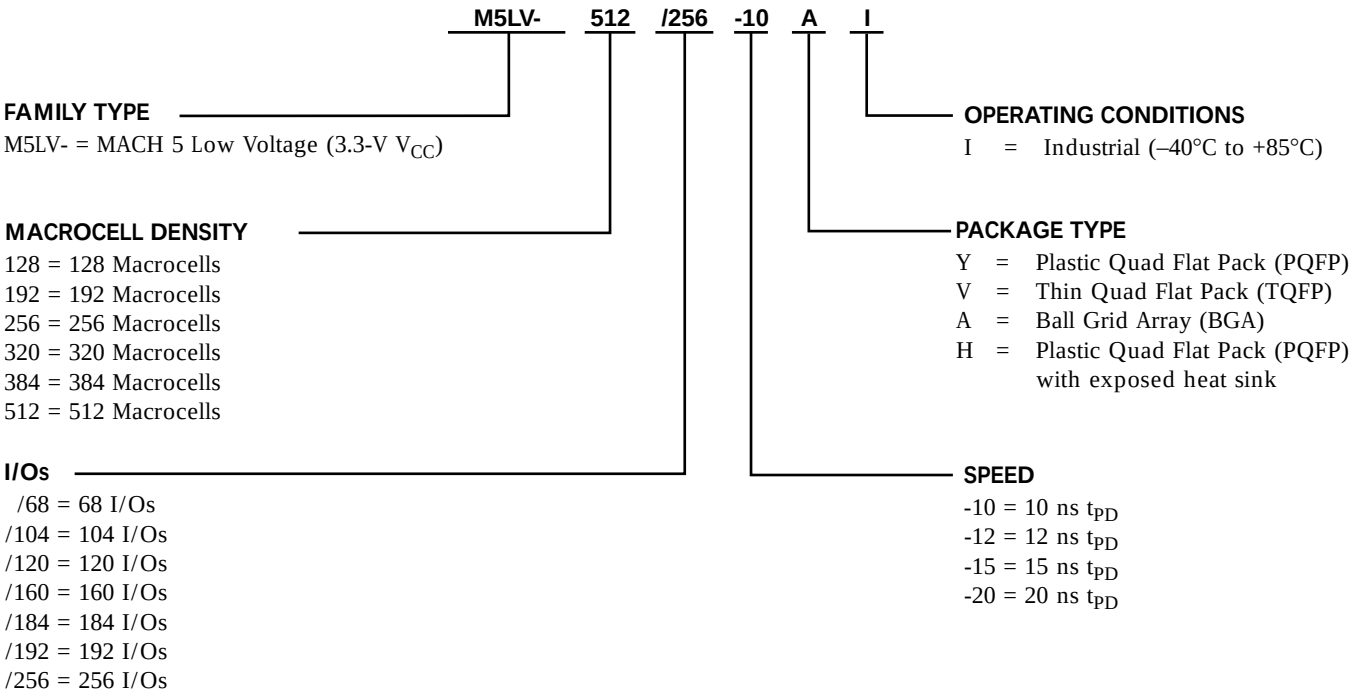
**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

# ORDERING INFORMATION

## MACH 5 LV IND -10, -12, -15, -20

Vantis standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.




| Valid Combinations | | |
|---|---|---|
| M5LV-128/68 | -10, -12, -15, -20 | YI, VI |
| M5LV-128/104 | | YI |
| M5LV-128/120 | | YI |
| M5LV-192/68 | | YI, VI |
| M5LV-192/104 | | YI |
| M5LV-192/120 | | YI |
| M5LV-192/160 | | YI |
| M5LV-256/68 | | YI, VI |
| M5LV-256/104 | | YI |
| M5LV-256/120 | | YI |
| M5LV-256/160 | | YI |

### Device Marking

Actual device marking differs from the ordering part number (OPN). “MACH 5” is marked on a device wherever “M5-” is used in the OPN.

| Valid Combinations | | |
|---|---|---|
| M5LV-320/120 | -10, -12, -15, -20 | HI |
| M5LV-320/160 | | HI |
| M5LV-320/184 | | HI |
| M5LV-320/192 | | AI |
| M5LV-384/120 | | HI |
| M5LV-384/160 | | HI |
| M5LV-384/184 | | HI |
| M5LV-384/192 | | AI |
| M5LV-512/120 | | HI |
| M5LV-512/160 | | HI |
| M5LV-512/184 | | HI |
| M5LV-512/192 | | AI |
| M5LV-512/256 | | AI |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## FUNCTIONAL DESCRIPTION

The Fifth Generation MACH Architecture yields the highest speeds at the highest CPLD densities. Extensive routing resources ensure pinout retention as well as high utilization. The MACH 5 architecture consists of PAL blocks connected by two levels of interconnect. Each group of four PAL blocks is given its own routing resources, called **block interconnect**. Together, the four PAL blocks and their block interconnect are called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together (see Figure 1). The only logic difference between any two MACH 5 devices is the number of segments, so once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four pin clocks available which can also be used as logic inputs.

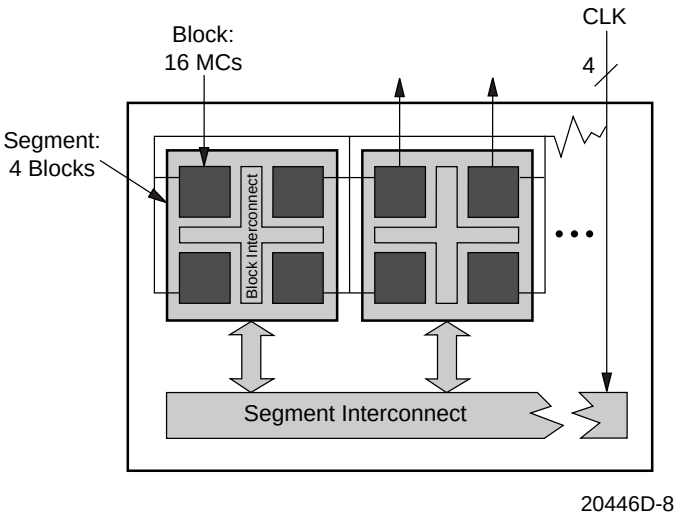



**Figure 1. MACH 5 Block Diagram with Segment Numbers**

### Enhanced PAL Block

The MACH 5 PAL blocks consist of the elements listed below. While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- Macrocell
- Logic array
- Logic allocator
- I/O cell
- Register control generator
- Output enable generator

The I/Os associated with each PAL block (Figure 2) have a path directly back to that PAL block called **local feedback**. If the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnect provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs. Two inputs per PAL block can also be fed directly to a macrocell for registered input applications.

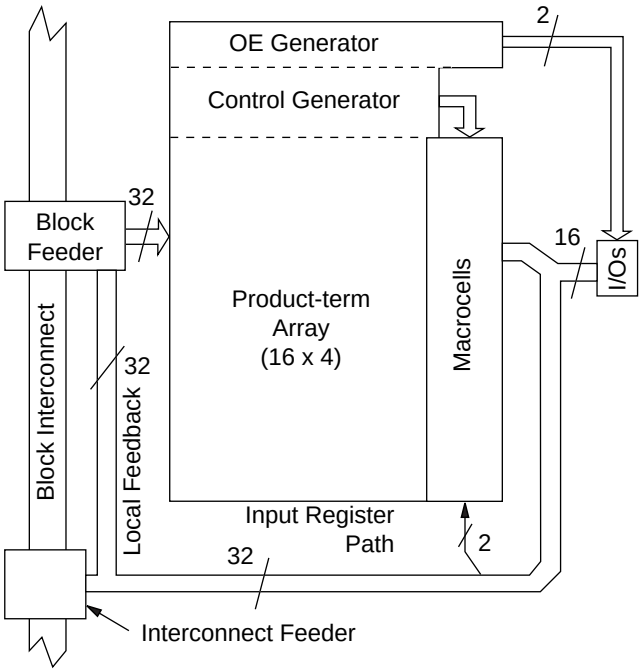



**Figure 2. PAL Block Structure**

## Logic Array and Allocator

The product-term array has the familiar sum-of-products architecture used in PAL devices. The logic allocator assigns product terms to macrocells. Up to eight clusters of four product terms can be steered to one macrocell, and product terms can be steered in a basic cluster of three or four product terms. If three product terms are steered away, one can be left for separate logic generation. The logic allocator acts as an output logic switch matrix: as a design changes, the **logic allocator** will reassign logic to macrocells to retain pinout. If not used in a cluster, the extra product term can be XORed with the basic cluster for functions such as data comparison. If the basic cluster of three product terms is steered away, the product term remaining can still be used for logic generation. The XOR gate available to each macrocell can be used for logic and/or for polarity control. The product term clusters available to each macrocell within a PAL block are shown in Table 3.

Rather than an output switch matrix which reassigns macrocells to pins to retain pinout, the wide logic allocator produces the same result by reassigning logic to macrocells. In addition, large equations (up to 32 product terms) can be implemented in a MACH 5 device with only one pass through the logic array.

**Table 3. Product Term Steering Options for PT Clusters and Macrocells**

| Macrocell | Available Clusters | Macrocell | Available Clusters |
|---|---|---|---|
| $M_0$ | $C_0$, $C_1$, $C_2$, $C_3$, $C_4$ | $M_8$ | $C_5$, $C_6$, $C_7$, $C_8$, $C_9$, $C_{10}$, $C_{11}$, $C_{12}$ |
| $M_1$ | $C_0$, $C_1$, $C_2$, $C_3$, $C_4$, $C_5$ | $M_9$ | $C_6$, $C_7$, $C_8$, $C_9$, $C_{10}$, $C_{11}$, $C_{12}$, $C_{13}$ |
| $M_2$ | $C_0$, $C_1$, $C_2$, $C_3$, $C_4$, $C_5$, $C_6$ | $M_{10}$ | $C_7$, $C_8$, $C_9$, $C_{10}$, $C_{11}$, $C_{12}$, $C_{13}$, $C_{14}$ |
| $M_3$ | $C_0$, $C_1$, $C_2$, $C_3$, $C_4$, $C_5$, $C_6$, $C_7$ | $M_{11}$ | $C_8$, $C_9$, $C_{10}$, $C_{11}$, $C_{12}$, $C_{13}$, $C_{14}$, $C_{15}$ |
| $M_4$ | $C_0$, $C_1$, $C_2$, $C_3$, $C_4$, $C_5$, $C_6$, $C_7$ | $M_{12}$ | $C_8$, $C_9$, $C_{10}$, $C_{11}$, $C_{12}$, $C_{13}$, $C_{14}$, $C_{15}$ |
| $M_5$ | $C_1$, $C_2$, $C_3$, $C_4$, $C_5$, $C_6$, $C_7$, $C_8$ | $M_{13}$ | $C_9$, $C_{10}$, $C_{11}$, $C_{12}$, $C_{13}$, $C_{14}$, $C_{15}$ |
| $M_6$ | $C_2$, $C_3$, $C_4$, $C_5$, $C_6$, $C_7$, $C_8$, $C_9$ | $M_{14}$ | $C_{10}$, $C_{11}$, $C_{12}$, $C_{13}$, $C_{14}$, $C_{15}$ |
| $M_7$ | $C_3$, $C_4$, $C_5$, $C_6$, $C_7$, $C_8$, $C_9$, $C_{10}$ | $M_{15}$ | $C_{11}$, $C_{12}$, $C_{13}$, $C_{14}$, $C_{15}$ |

## Macrocells

The macrocells for MACH 5 consist of a storage element, a control (clock and set or reset or latch enable) bus, and routing resources. The macrocell (Figure 3) can be configured for combinatorial, registered or latched operation. The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

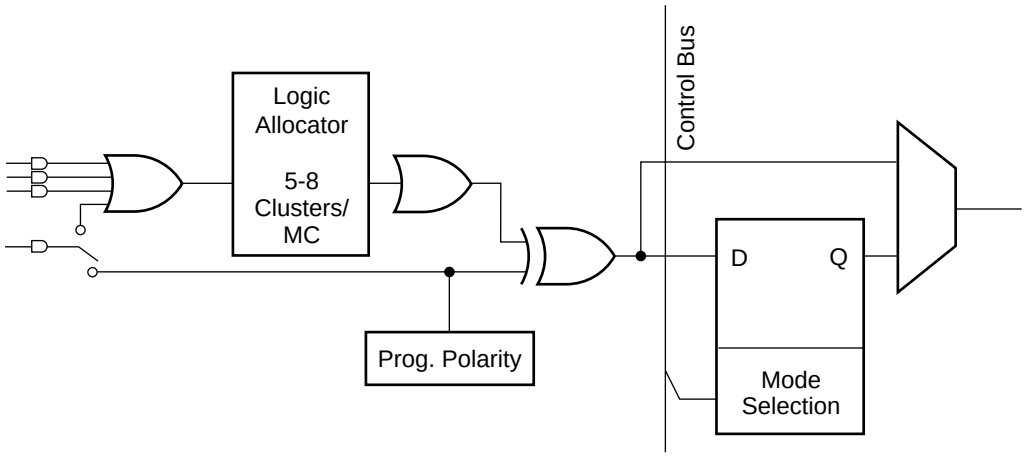



**Figure 3. Macrocell Diagram**

## Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines (Figure 4) provide synchronous global (pin) clocks and asynchronous product term clocks, sum term clocks, and latch enables. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

### Clock Line 0 Options

- Global clock (0, 1, 2, or 3) with positive or negative edge clock enable
- Product-term clock (A*B*C)
- Sum-term clock (A+B+C)

### Clock Line 1 Options

- Global clock (0, 1, 2, or 3) with positive edge clock enable
- Global clock (0, 1, 2, or 3) with negative edge clock enable
- Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

### Clock Line 2 Options

- Global clock (0, 1, 2, or 3) with clock enable

### Clock Line 3 Options

- Complement of clock line 2 (same clock enable)
- Product-term clock (if clock line 2 does not use clock enable

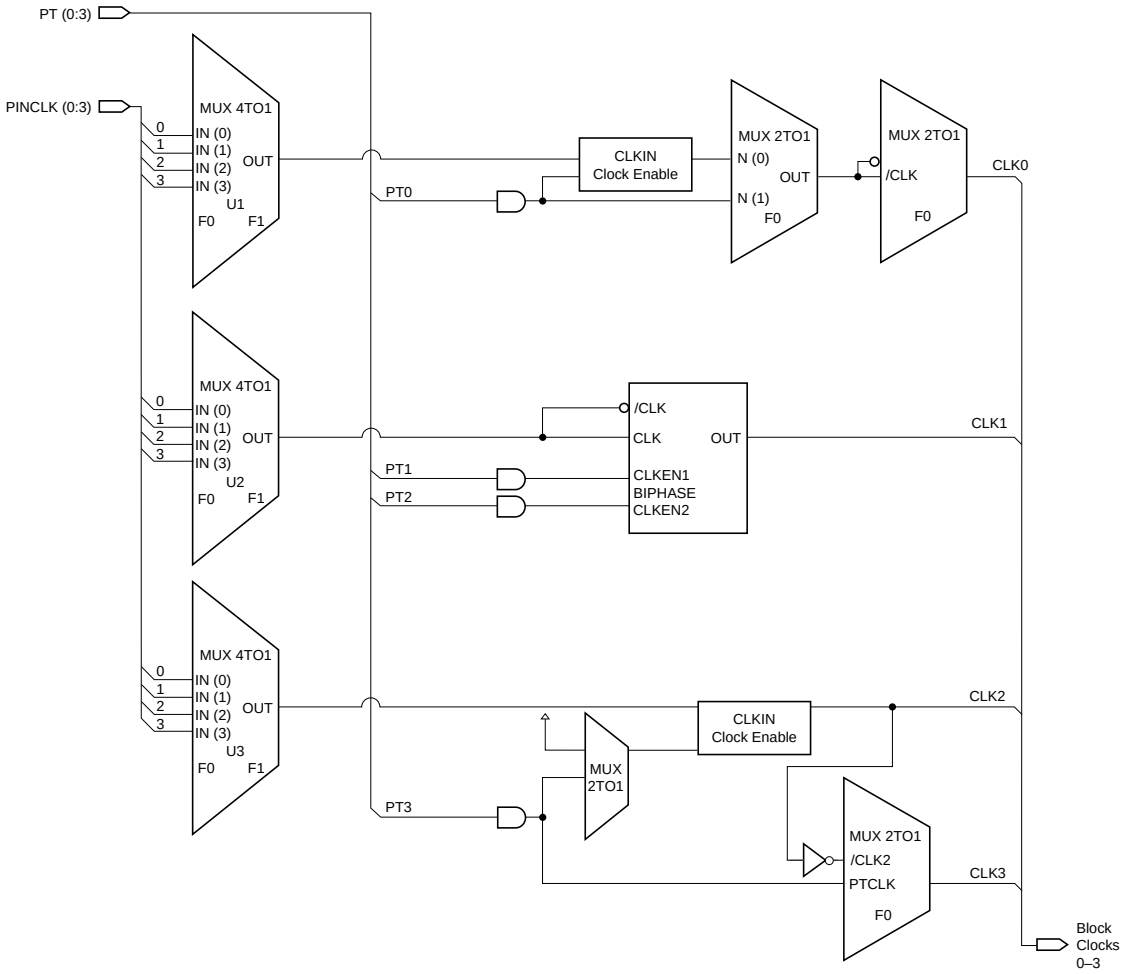



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**Figure 4. Clock Generator**

Three of the four global clocks are available within any given PAL block. There are two product-term clocks and one sum-term clock available per PAL block.

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

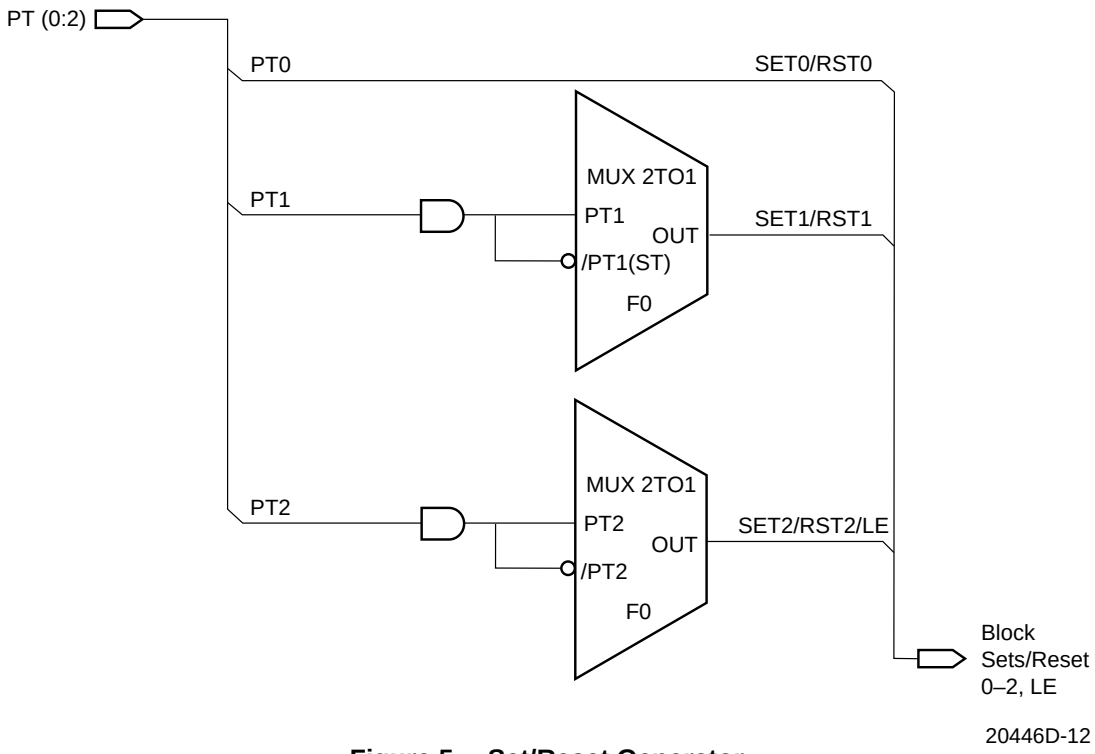


**Figure 5. Set/Reset Generator**

## OE Generator

There is one output enable (OE) generator per PAL block that generates two product-term driven output enables. Each I/O cell is simply an output buffer. Each macrocell within the PAL block can choose to be permanently enabled, permanently disabled, or choose one of the two product term output enables per PAL block (Figure 6).

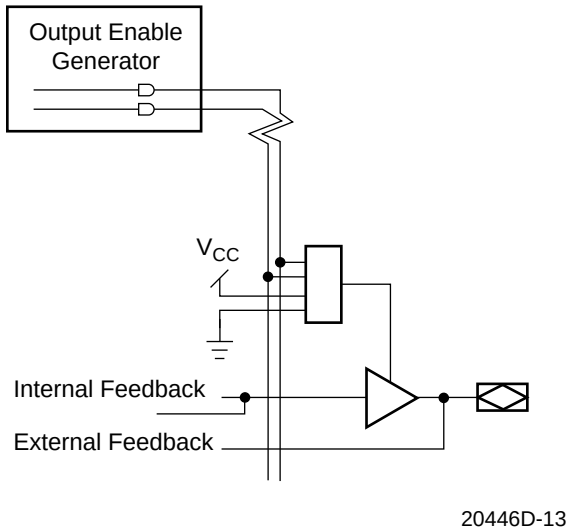


**Figure 6. Output Enable Generator and I/O Cell**

# MACH 5 TIMING

MACH 5 timing can be modeled on any Vantis approved software tool or it can be estimated using the model shown in Figure 7. For more information, please see the application note *MACH 5 Timing Considerations.* Device timing will depend on the level of interconnect used and the power level chosen for a particular path. These are the path and power factors. The pin-to-pin delays can be

calculated by following one path from input/feedback to output. For example, $t_{PD}$ is the pin-to-pin delay for a signal within a PAL block. $t_{PD}+t_{BLK}$ is the pin-to-pin delay for a signal that uses the block interconnect and stays within a segment. $t_{PD}+t_{SEG}$ is the pin-to-pin delay for a signal that uses both the block and segment interconnect. Power level timing is calculated in the same manner. If a signal uses block interconnect and is placed in a low-power block, then the pin-to-pin delay will be $t_{PD}+t_{BLK}+t_{PL3}$.

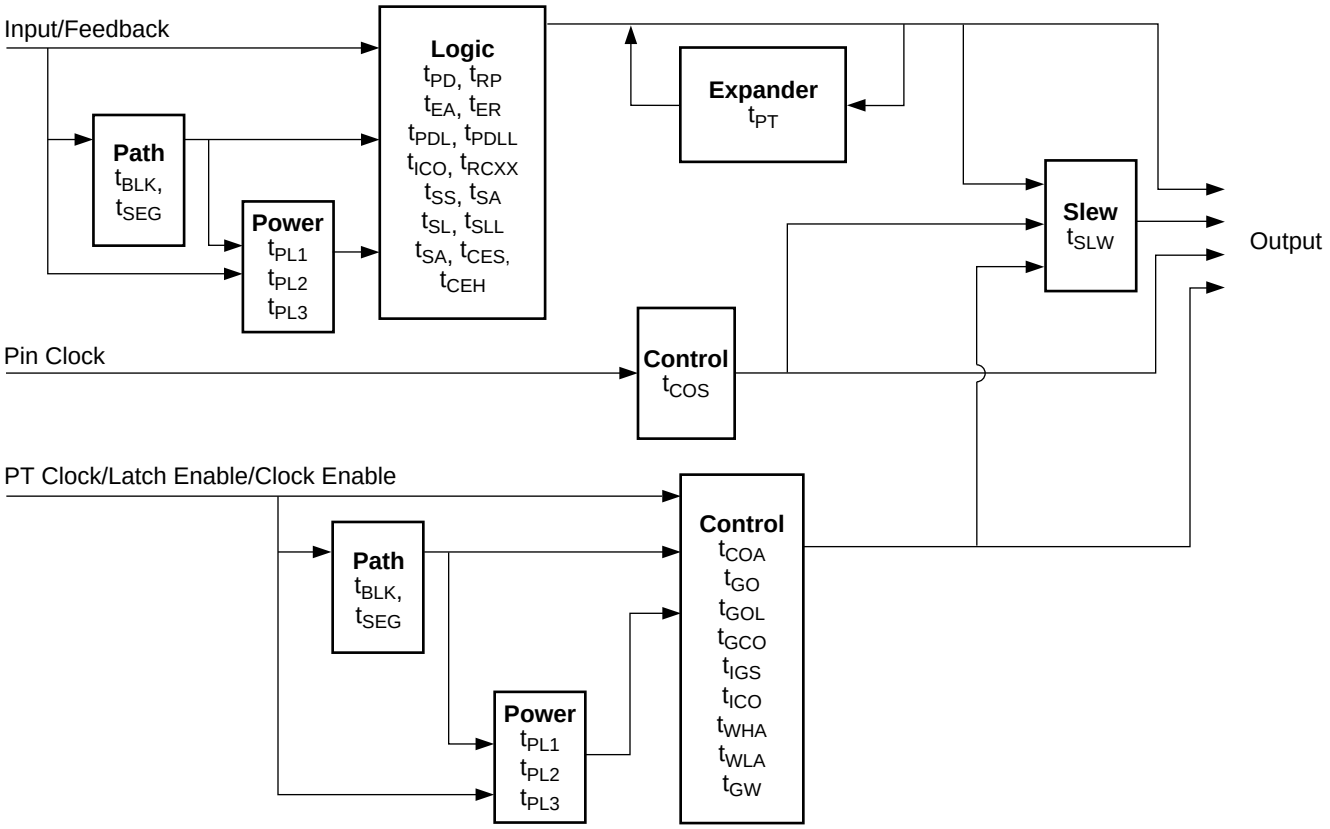


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**Figure 7. MACH 5 Timing Factors**

## JTAG, IN-SYSTEM PROGRAMMING

All MACH 5 devices are in-system programmable and are compliant to the JTAG standard, IEEE 1149.1, developed for checking circuit board connectivity. MACH in-system programming is implemented as an extension of this standard which uses manufacturer defined instructions and registers for program and verify. In-system programming eases prototyping and reduces manufacturing steps. The MACH 5 devices can be programmed across the commercial temperature range. Minimum programming time is typically less than 5 seconds. Vantis' MACHPRO software serializes JEDEC files and downloads them to the target board through the PC parallel port. The MACH 5 devices can be programmed in any JTAG chain.

## PCI COMPLIANT

The MACH 5 family members in the -7/-10/-12 speeds are fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group (SIG). The MACH 5 devices provide the speed, drive, density and I/Os for the most complex PCI designs.

## SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

All MACH 5 devices have both 3.3-V and 5-V $V_{CC}$ versions available. Both versions are safe for mixed supply voltage system designs. The 5-V device will not overdrive 3.3-V devices above the output voltage of 3.3 V, while it accepts inputs from other 3.3-V devices. The 3.3-V device will accept inputs up to 5.5 V. Both the 5-V and 3.3-V versions have the same high-speed performance.

## BUS-FRIENDLY I/O STRUCTURE

All of the MACH 5 devices have a Bus-Friendly input structure which weakly holds an input at its last driven state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from threshold where noise can cause high-frequency switching.

## MULTIPLE I/O AND DENSITY OPTIONS

As logic needs change during the design process, the MACH 5 family offers six macrocell densities and seven I/O options to optimize cost and functionality concerns.

The MACH 5 family also offers the ability to fit a working design on a member device into another device with the same number of I/Os but a different macrocell density. With proper considerations during design, this feature will allow pins to be fixed in the same locations and require no board reconfiguration.

## POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block. The speed and power tradeoff can be tailored for each design. In large designs, there may be several different speed requirements for different portions of a design. In a computing design, a state machine controller may require the fastest speed available, while the data path portion may run at the slower speed of the bus.

**Table 4. Power Levels**

| | |
|---|---|
| High Speed/High Power | 100% power |
| Medium High Speed/Medium High Power | 67% power |
| Medium Low Speed/Medium Low Power | 40% power |
| Low Speed/low Power | 20% power |

## PROGRAMMABLE SLEW-RATE

Each MACH 5 I/O has an individual programmable slew-rate control bit. Each output can be configured for the highest speed (3 V/ns) or for the lowest noise (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections and less noise. For designs with short traces or well terminated lines, the fast-slew rate can be used to achieve the highest speed. The slew-rate is adjusted independent of power.

## POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the $V_{CC}$ rise must be monotonic and clock must be inactive until the reset delay time has elapsed.

## SECURITY

A programmable security bit is provided to prevent unauthorized copying of array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern, securing proprietary designs from competitors. The security bit can only be erased in conjunction with the array during an erase cycle.

## QUALITY AND TESTABILITY

The MACH 5 devices are electrically erasable which allows for full AC and DC verification of every device. In addition this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

## TECHNOLOGY

The MACH 5 devices are fabricated on AMD's own state-of-the-art 0.5 and 0.35 micron ($L_{eff}$) EECMOS technologies. This advanced technology allows MACH 5 to offer both the highest performance CPLDs and the lowest power CPLDs in the industry. The floating gate cells rely on Fowler-Nordheim tunneling to charge the gates, and have long proven their endurance and reliability.

The substrate of these devices is grounded to provide substrate clamp diodes on every input which makes inputs more immune to noisy input signals.

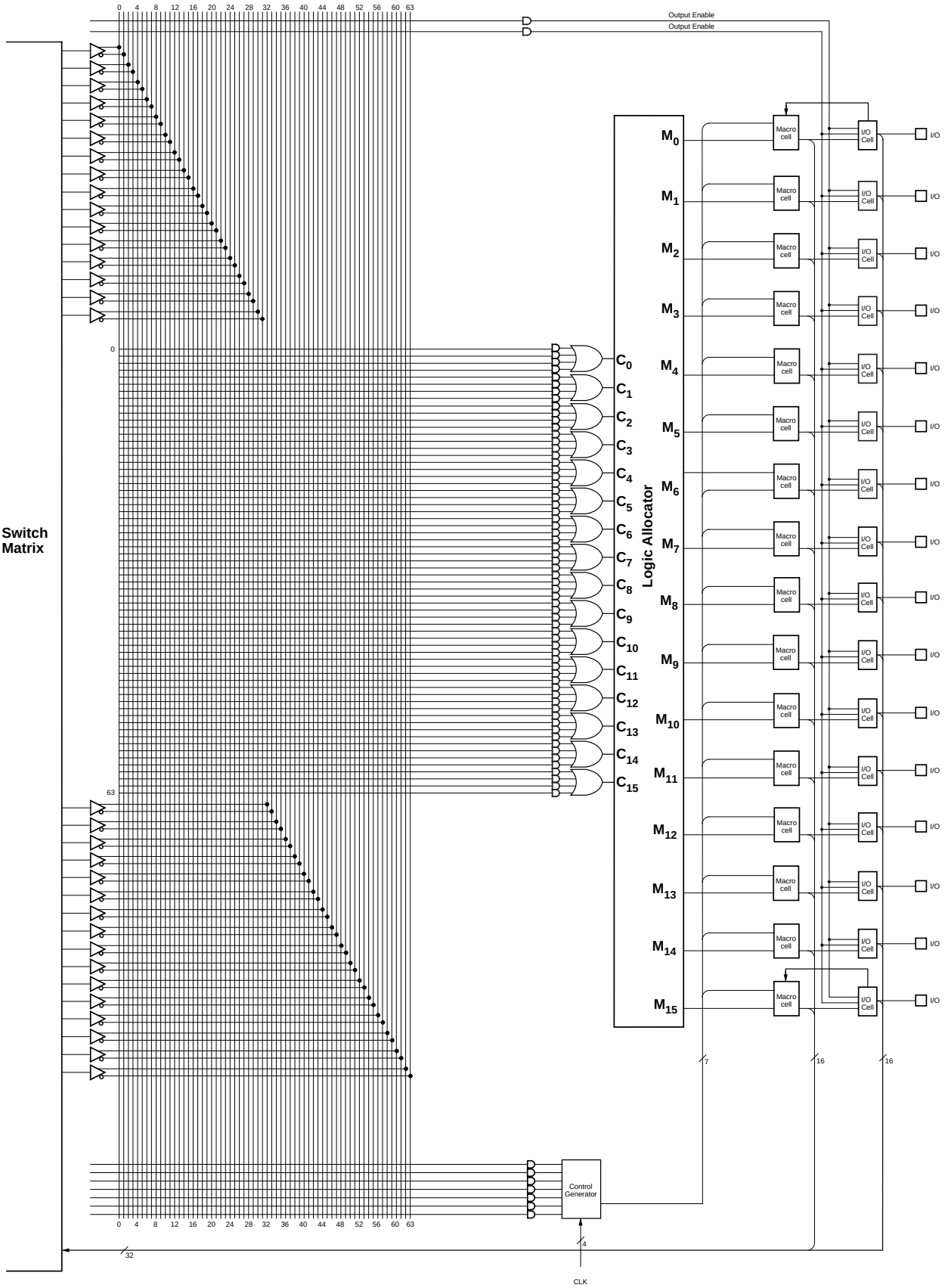


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**Figure 8. MACH 5 PAL Block**

## ABSOLUTE MAXIMUM RATINGS

### MACH 5 COM -7.5, -10, -12, -15

Storage Temperature . . . . . –65°C to +150°C

Device Junction Temperature . . . . . +130°C to +150°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . 0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (0°C to +70°C) . . . . . 200 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Ambient Temperature ($T_A$)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage ($V_{CC}$)
with Respect to Ground . . . . . +4.75 V to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## 5-V DC CHARACTERISTICS over COMMERCIAL operating ranges

| Parameter Symbol | Parameter Description | Test Description | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –3.2 mA, $V_{CC}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | 2.4 | 3.3 | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = +16 mA, $V_{CC}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 5.25, $V_{CC}$ = Max (Note 2) | | 10 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0, $V_{CC}$ = Max (Note 2) | | –10 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 5.25, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 10 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | –10 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 3) | –30 | –180 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ or $I_{IH}$ and $I_{OZH}$.*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | I/CLK pin | $V_{IN}$ = 2.0 V | 5 V, 25°C, 1 MHz | 12 | pF |
| $C_{I/O}$ | I/O pin | $V_{OUT}$ = 2.0 V | 5 V, 25°C, 1 MHz | 10 | pF |

***Note:***

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

### BASIC (all signals from within PAL block except global control signals)

| Parameter Symbol | Parameter Description | -7 | | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PD}$ | Input, I/O, or Feedback to Combinatorial Output | 2 | 7.5 | 2 | 10 | 2 | 12 | 2 | 15 | ns |
| $t_{SS}$ | Setup Time from Input, I/O, or Feedback to Global Clock | 4 | | 5 | | 6 | | 8 | | ns |
| $t_{HS}$ | Register Data Hold Time Using a Global Clock | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{COS}$ | Global Clock to Output (Pin Clock) | | 6 | | 7 | | 8 | | 10 | ns |
| $t_{WLS}$ | Global Clock Low Width (Note 3) | 3 | | 4 | | 5 | | 6 | | ns |
| $t_{WHS}$ | Global Clock High Width (Note 3) | 3 | | 4 | | 5 | | 6 | | ns |
| $f_{MAX}$ | External Feedback, PAL Block Level $1/(t_{SS} + t_{COS})$ | 100 | | 83 | | 71 | | 55 | | MHz |
| | Internal Feedback PAL Block Level | 125 | | 100 | | 83.3 | | 83.3 | | MHz |
| | No Feedback PAL Block Level | 166.7 | | 125 | | 100 | | 83.3 | | MHz |
| $t_{SA}$ | Setup Time from Input, I/O, or Feedback to Product Term Clock, PAL Block Level | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{HA}$ | Output Register Data Hold Time Using a Product Term Clock | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{COA}$ | Product Term Clock to Output | | 10 | | 12 | | 15 | | 17 | ns |
| $t_{WLA}$ | Product Term Clock Width LOW | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{WHA}$ | Product Term Clock Width HIGH | 4 | | 5 | | 6 | | 7 | | ns |
| $f_{MAXA}$ | External Feedback, PAL Block Level $1/(t_{SA} + t_{COA})$ | 71 | | 58 | | 47.6 | | 42 | | MHz |
| | Internal Feedback, PAL Block Level | 88 | | 72 | | 60 | | 52 | | MHz |
| | No Feedback, PAL Block Level | 125 | | 100 | | 83.3 | | 71.4 | | MHz |
| $t_{SL}$ | Setup Time from Input, I/O, or Feedback to Product Term Gate | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{HL}$ | Latch Data Hold Time (Using Product Term Gate) | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{GO}$ | Latch Gate to Output | | 10 | | 11 | | 12 | | 13 | ns |
| $t_{GOL}$ | Latch Gate to Output through Transparent Latch | | 17 | | 18 | | 19 | | 20 | ns |

## BASIC (all signals from within PAL block except global control signals) (Continued)

| Parameter Symbol | Parameter Description | -7 | | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{GCO}$ | Latch Gate to Combinatorial Output | | 17 | | 18 | | 19 | | 20 | ns |
| $t_{IGS}$ | Latch Gate to Output Latch Setup | 10 | | 11 | | 12 | | 13 | | ns |
| $t_{GW}$ | Gate Width LOW (for LOW Transparent) or High (for HIGH Transparent) | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{BUF}$ | Delay Savings for Using Internal Feedback Instead of Pin Feedback (I/Os Only, No Savings for Buried) | 0.5 | 2 | 0.5 | 2 | 0.5 | 2 | 0.5 | 2 | ns |

## ASYNCHRONOUS SET and RESET, OUTPUT ENABLE, CLOCK ENABLE

| Parameter Symbol | Parameter Description | -7 | | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RP}$ | Asynchronous Reset or Preset to Registered or Latched Output | | 10 | | 12 | | 14 | | 16 | ns |
| $t_{PRW}$ | Asynchronous Reset or Preset Width | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{PRR}$ | Asynchronous Reset or Preset Recovery Time | 7.5 | | 8 | | 9 | | 10 | | ns |
| $t_{EA}$ | Input, I/O, or Feedback to Output Enable | 2 | 9.5 | 2 | 10 | 2 | 12 | 2 | 15 | ns |
| $t_{ER}$ | Input, I/O, or Feedback to Output Disable | | 9.5 | | 10 | | 12 | | 15 | ns |
| $t_{CES}$ | Setup Time from Clock Enable to Next Clock Pulse | 4 | | 5 | | 7 | | 7 | | ns |
| $t_{CEH}$ | Hold Time for Clock Enable After Last Enabled Clock Pulse | 4 | | 5 | | 6 | | 6 | | ns |
| $t_{RCEH}$ | Hold Time for Registered Clock Enable After Last Enabled Clock Pulse | 0 | | 0 | | 0 | | 0 | | ns |

## REGISTERS and LATCHES (input and output, BLOCK level)

| Parameter Symbol | Parameter Description | -7 | | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PDIL}$ | Input, I/O, or Feedback to Output Through Transparent Input Latch | | 13 | | 15 | | 17 | | 19 | ns |
| $t_{ICOG}$ | Input Register Global Clock to Combinatorial Output | | 13 | | 14 | | 16 | | 18 | ns |
| $t_{ICOA}$ | Input Register Product Term Clock to Combinatorial Output | | 17 | | 18 | | 19 | | 20 | ns |
| $t_{SIRS}$ | Input Register Setup Time Using Global Clock | 2 | | 3 | | 3 | | 3 | | ns |
| $t_{SIRA}$ | Input Register Setup Time Using Product Term Clock | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HIRS}$ | Input Register Hold Time Using Global Clock | 3 | | 4 | | 4 | | 4 | | ns |
| $t_{HIRA}$ | Input Register Hold Time Using Product Term Clock | 6 | | 7 | | 7 | | 7 | | ns |
| $t_{WICW}$ | Input Register Clock Width Low or High | 4 | | 5 | | 6 | | 7 | | ns |
| $f_{MAXI}$ | Maximum Input Register Frequency | 125 | | 100 | | 83.3 | | 71.4 | | MHz |
| $t_{RCSS}$ | Register Using Global Clock to Output Register Using Global Clock Setup Time | 9.5 | | 12 | | 14 | | 17 | | ns |
| $t_{RCSA}$ | Register Using Global Clock to Output Register Using Product Term Clock Setup Time | 12.5 | | 15 | | 17 | | 18 | | ns |
| $t_{RCAS}$ | Register Using Product Term Clock to Output Register Using Global Clock Setup Time | 12.5 | | 15 | | 17 | | 18 | | ns |
| $t_{RCAA}$ | Register Using Product Term Clock to Output Register Using Same Product Term Clock Setup Time | 10 | | 10 | | 12 | | 15 | | ns |
| $t_{SIL}$ | Input Latch Setup Time | 2 | | 3 | | 3 | | 3 | | ns |
| $t_{HIL}$ | Input Latch Hold Time | 6 | | 7 | | 7 | | 7 | | ns |
| $t_{SLL}$ | Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate | 9 | | 10 | | 11 | | 12 | | ns |
| $t_{PDLL}$ | Input, I/O, or Feedback to Output Through Transparent Input and Output Latches | | 14 | | 16 | | 18 | | 20 | ns |

## INTERCONNECT

| Parameter Symbol | Parameter Description | -7 | | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{BLK}$ | Interconnect delay between blocks. If a signal depends on inputs not in the same block, but in the same segment, this delay must be added to $t_{PD}$, $t_{SS}$, $t_{SA}$, $t_{COA}$, $t_{SL}$, $t_{GO}$, $t_{GOL}$, $t_{GCO}$, $t_{IGS}$, $t_{RP}$, $t_{EA}$, $t_{ER}$, $t_{CES}$, $t_{PDL}$, $t_{ICO}$, $t_{RCSS}$, $t_{RCAS}$, $t_{RCAA}$, $t_{PDLL}$, $t_{SLL}$. | | 1.5 | | 2.0 | | 2.0 | | 2.0 | ns |
| $t_{SEG}$ | Interconnect delay between segments. This parameter includes all block interconnect delay. If a signal depends on inputs not in the same segment, this delay must be added to $t_{PD}$, $t_{SS}$, $t_{SA}$, $t_{COA}$, $t_{SL}$, $t_{GO}$, $t_{GOL}$, $t_{GCO}$, $t_{IGS}$, $t_{RP}$, $t_{EA}$, $t_{ER}$, $t_{CES}$, $t_{PDL}$, $t_{ICO}$, $t_{RCSS}$, $t_{RCAS}$, $t_{RCAA}$, $t_{PDLL}$, $t_{SLL}$. | | 5 | | 6.0 | | 6.0 | | 6.0 | ns |

## POWER, LOGIC, AND SLEW (Please see individual device data sheets for details.)

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies (Fmax/2).*

## ABSOLUTE MAXIMUM RATINGS

### MACH 5 LV COM -7.5, -10, -12, -15

Storage Temperature . . . . . –65°C to +150°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . 0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (0°C to +70°C) . . . . . 200 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Ambient Temperature ($T_A$)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage ($V_{CC}$)
with Respect to Ground . . . . . +3.0 V to +3.6 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## 3.3-V DC CHARACTERISTICS over COMMERCIAL operating ranges

| Parameter Symbol | Parameter Description | Test Description | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –100 µA | $V_{CC}$ –0.2 | | V |
| | | | $I_{OH}$ = 3.2 mA | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 100 µA | | 0.2 | V |
| | | | $I_{OH}$ = 16 mA (Note 1) | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 2) | | 2.0 | 5.5 | V |
| $V_{IL}$ | Input LOW Voltage | $V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 2) | | –0.3 | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 3.6, $V_{CC}$ = Max (Note 3) | | | 5 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0, $V_{CC}$ = Max (Note 3) | | | –5 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 3.6, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 3) | | | 5 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 3) | | | –5 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | –15 | –160 | mA |

***Notes:***

1. *Total $I_{OL}$ for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
3. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ or $I_{IH}$ and $I_{OZH}$.*
4. *Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | I/CLK pin | $V_{IN}$ = 2.0 V | 3.3 V, 25°C, 1 MHz | 12 | pF |
| $C_{I/O}$ | I/O pin | $V_{OUT}$ = 2.0 V | 3.3 V, 25°C, 1 MHz | 10 | pF |

***Note:***

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

### BASIC (all signals from within PAL block except global control signals)

| Parameter Symbol | Parameter Description | -7 | | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PD}$ | Input, I/O, or Feedback to Combinatorial Output | 2 | 7.5 | 2 | 10 | 2 | 12 | 2 | 15 | ns |
| $t_{SS}$ | Setup Time from Input, I/O, or Feedback to Global Clock | 4 | | 5 | | 6 | | 8 | | ns |
| $t_{HS}$ | Register Data Hold Time Using a Global Clock | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{COS}$ | Global Clock to Output (Pin Clock) | | 6 | | 7 | | 8 | | 10 | ns |
| $t_{WLS}$ | Global Clock Low Width (Note 3) | 3 | | 4 | | 5 | | 6 | | ns |
| $t_{WHS}$ | Global Clock High Width (Note 3) | 3 | | 4 | | 5 | | 6 | | ns |
| $f_{MAX}$ | External Feedback, PAL Block Level $1/(t_{SS} + t_{COS})$ | 100 | | 83 | | 71 | | 55 | | MHz |
| | Internal Feedback PAL Block Level | 125 | | 100 | | 83.3 | | 83.3 | | MHz |
| | No Feedback PAL Block Level | 166.7 | | 125 | | 100 | | 83.3 | | MHz |
| $t_{SA}$ | Setup Time from Input, I/O, or Feedback to Product Term Clock, PAL Block Level | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{HA}$ | Output Register Data Hold Time Using a Product Term Clock | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{COA}$ | Product Term Clock to Output | | 10 | | 12 | | 15 | | 17 | ns |
| $t_{WLA}$ | Product Term Clock Width LOW | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{WHA}$ | Product Term Clock Width HIGH | 4 | | 5 | | 6 | | 7 | | ns |
| $f_{MAXA}$ | External Feedback, PAL Block Level $1/(t_{SA} + t_{COA})$ | 71 | | 58 | | 47.6 | | 42 | | MHz |
| | Internal Feedback, PAL Block Level | 88 | | 72 | | 60 | | 52 | | MHz |
| | No Feedback, PAL Block Level | 125 | | 100 | | 83.3 | | 71.4 | | MHz |
| $t_{SL}$ | Setup Time from Input, I/O, or Feedback to Product Term Gate | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{HL}$ | Latch Data Hold Time (Using Product Term Gate) | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{GO}$ | Latch Gate to Output | | 10 | | 11 | | 12 | | 13 | ns |
| $t_{GOL}$ | Latch Gate to Output through Transparent Latch | | 17 | | 18 | | 19 | | 20 | ns |

## BASIC (all signals from within PAL block except global control signals) (Continued)

| Parameter Symbol | Parameter Description | -7 | | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{GCO}$ | Latch Gate to Combinatorial Output | | 17 | | 18 | | 19 | | 20 | ns |
| $t_{IGS}$ | Latch Gate to Output Latch Setup | 10 | | 11 | | 12 | | 13 | | ns |
| $t_{GW}$ | Gate Width LOW (for LOW Transparent) or High (for HIGH Transparent) | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{BUF}$ | Delay Savings for Using Internal Feedback Instead of Pin Feedback (I/Os Only, No Savings for Buried) | 0.5 | 2 | 0.5 | 2 | 0.5 | 2 | 0.5 | 2 | ns |

## ASYNCHRONOUS SET and RESET, OUTPUT ENABLE, CLOCK ENABLE

| Parameter Symbol | Parameter Description | -7 | | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RP}$ | Asynchronous Reset or Preset to Registered or Latched Output | | 10 | | 12 | | 14 | | 16 | ns |
| $t_{PRW}$ | Asynchronous Reset or Preset Width | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{PRR}$ | Asynchronous Reset or Preset Recovery Time | 7.5 | | 8 | | 9 | | 10 | | ns |
| $t_{EA}$ | Input, I/O, or Feedback to Output Enable | 2 | 9.5 | 2 | 10 | 2 | 12 | 2 | 15 | ns |
| $t_{ER}$ | Input, I/O, or Feedback to Output Disable | | 9.5 | | 10 | | 12 | | 15 | ns |
| $t_{CES}$ | Setup Time from Clock Enable to Next Clock Pulse | 5 | | 6 | | 7 | | 7 | | ns |
| $t_{CEH}$ | Hold Time for Clock Enable Following Last Enabled Clock Pulse | 4 | | 5 | | 6 | | 6 | | ns |
| $t_{RCEH}$ | Hold Time for Registered Clock Enable After Last Enabled clock Edge | 0 | | 0 | | 0 | | 0 | | ns |

## REGISTERS and LATCHES (input and output, BLOCK level)

| Parameter Symbol | Parameter Description | -7 | | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PDIL}$ | Input, I/O, or Feedback to Output Through Transparent Input Latch | | 13 | | 15 | | 17 | | 19 | ns |
| $t_{ICOG}$ | Input Register Global Clock to Combinatorial Output | | 13 | | 14 | | 16 | | 18 | ns |
| $t_{ICOA}$ | Input Register Product Term Clock to Combinatorial Output | | 17 | | 18 | | 19 | | 20 | ns |
| $t_{SIRS}$ | Input Register Setup Time Using Global Clock | 2 | | 3 | | 3 | | 3 | | ns |
| $t_{SIRA}$ | Input Register Setup Time Using Product Term Clock | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HIRS}$ | Input Register Hold Time Using Global Clock | 3 | | 4 | | 4 | | 4 | | ns |
| $t_{HIRA}$ | Input Register Hold Time Using Product Term Clock | 6 | | 7 | | 7 | | 7 | | ns |
| $t_{WICW}$ | Input Register Clock Width Low or High | 4 | | 5 | | 6 | | 7 | | ns |
| $f_{MAXI}$ | Maximum Input Register Frequency | 125 | | 100 | | 83.3 | | 71.4 | | MHz |
| $t_{RCSS}$ | Register Using Global Clock to Output Register Using Global Clock Setup Time | 9.5 | | 12 | | 14 | | 17 | | ns |
| $t_{RCSA}$ | Register Using Global Clock to Output Register Using Product Term Clock Setup Time | 12.5 | | 15 | | 17 | | 18 | | ns |
| $t_{RCAS}$ | Register Using Product Term Clock to Output Register Using Global Clock Setup Time | 12.5 | | 15 | | 17 | | 18 | | ns |
| $t_{RCAA}$ | Register Using Product Term Clock to Output Register Using Same Product Term Clock Setup Time | 10 | | 10 | | 12 | | 15 | | ns |
| $t_{SIL}$ | Input Latch Setup Time | 2 | | 3 | | 3 | | 3 | | ns |
| $t_{HIL}$ | Input Latch Hold Time | 6 | | 7 | | 7 | | 7 | | ns |
| $t_{SLL}$ | Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate | 9 | | 10 | | 11 | | 12 | | ns |
| $t_{PDLL}$ | Input, I/O, or Feedback to Output Through Transparent Input and Output Latches | | 14 | | 16 | | 18 | | 20 | ns |

## INTERCONNECT

| Parameter Symbol | Parameter Description | -7 | | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{BLK}$ | Interconnect delay between blocks. If a signal depends on inputs not in the same block, but in the same segment, this delay must be added to $t_{PD}$, $t_{SS}$, $t_{SA}$, $t_{COA}$,$t_{SL}$, $t_{GO}$, $t_{GOL}$, $t_{GCO}$, $t_{IGS}$, $t_{RP}$, $t_{EA}$, $t_{ER}$, $t_{CES}$, $t_{PDL}$, $t_{ICO}$, $t_{RCSS}$, $t_{RCAS}$, $t_{RCAA}$, $t_{PDLL}$, $t_{SLL}$. | | 1.5 | | 2 | | 2 | | 2 | ns |
| $t_{SEG}$ | Interconnect delay between segments. This parameter includes all block interconnect delays. If a signal depends on inputs not in the same segment, this delay must be added to $t_{PD}$, $t_{SS}$, $t_{SA}$, $t_{COA}$, $t_{SL}$, $t_{GO}$, $t_{GOL}$, $t_{GCO}$, $t_{IGS}$, $t_{RP}$, $t_{EA}$, $t_{ER}$, $t_{CES}$, $t_{PDL}$, $t_{ICO}$, $t_{RCSS}$, $t_{RCAS}$, $t_{RCAA}$, $t_{PDLL}$, $t_{SLL}$. | | 5 | | 6 | | 6 | | 6 | ns |

## POWER, LOGIC, AND SLEW (Please see individual device data sheets for details.)

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies (Fmax/2).*

## ABSOLUTE MAXIMUM RATINGS

### MACH 5 IND -10, -12, -15, -20

Storage Temperature . . . . . –65°C to +150°C

Device Junction Temperature . . . . . +130°C to +150°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . 0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (–40°C to +85°C) . . . . . 200 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Ambient Temperature ($T_A$)
Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage ($V_{CC}$)
with Respect to Ground . . . . . +4.5 V to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## 5-V DC CHARACTERISTICS over INDUSTRIAL operating ranges

| Parameter Symbol | Parameter Description | Test Description | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –3.2 mA, $V_{CC}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | 2.4 | 3.3 | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = +16 mA, $V_{CC}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 5.25, $V_{CC}$ = Max (Note 2) | | 10 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0, $V_{CC}$ = Max (Note 2) | | –10 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 5.25, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 10 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | –10 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 3) | –30 | –180 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ or $I_{IH}$ and $I_{OZH}$.*
3. *Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | I/CLK pin | $V_{IN}$ = 2.0 V | 5 V, 25°C, 1 MHz | 12 | pF |
| $C_{I/O}$ | I/O pin | $V_{OUT}$ = 2.0 V | 5 V, 25°C, 1 MHz | 10 | pF |

***Note:***

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

## SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

### BASIC (all signals from within PAL block except global control signals)

| Parameter Symbol | Parameter Description | -10 | | -12 | | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PD}$ | Input, I/O, or Feedback to Combinatorial Output or Input, I/O, or Feedback to Output through Transparent Output Latch | 2 | 10 | 2 | 12 | 2 | 15 | 2 | 20 | ns |
| $t_{SS}$ | Setup Time from Input, I/O, or Feedback to Global Clock | 5 | | 6 | | 8 | | 10 | | ns |
| $t_{HS}$ | Register Data Hold Time Using a Global Clock | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{COS}$ | Global Clock to Output (Pin Clock) | | 7 | | 8 | | 10 | | 12 | ns |
| $t_{WLS}$ | Global Clock Low Width (Note 3) | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{WHS}$ | Global Clock High Width (Note 3) | 4 | | 5 | | 6 | | 7 | | ns |
| $f_{MAX}$ | External Feedback, PAL Block Level $1/(t_{SS} + t_{COS})$ | 83 | | 71 | | 55 | | 45.5 | | MHz |
| | Internal Feedback PAL Block Level | 100 | | 83.3 | | 83.3 | | 71.4 | | MHz |
| | No Feedback PAL Block Level | 125 | | 100 | | 83.3 | | 71.4 | | MHz |
| $t_{SA}$ | Setup Time from Input, I/O, or Feedback to Product Term Clock, PAL Block Level | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{HA}$ | Output Register Data Hold Time Using a Product Term Clock | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{COA}$ | Product Term Clock to Output | | 12 | | 15 | | 17 | | 20 | ns |
| $t_{WLA}$ | Product Term Clock Width LOW | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{WHA}$ | Product Term Clock Width HIGH | 5 | | 6 | | 7 | | 8 | | ns |
| $f_{MAXA}$ | External Feedback, PAL Block Level $1/(t_{SA} + t_{COA})$ | 58 | | 47.6 | | 42 | | 35 | | MHz |
| | Internal Feedback, PAL Block Level | 72 | | 60 | | 52 | | 45 | | MHz |
| | No Feedback, PAL Block Level | 100 | | 83.3 | | 71.4 | | 62.5 | | MHz |
| $t_{SL}$ | Setup Time from Input, I/O, or Feedback to Product Term Gate | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{HL}$ | Latch Data Hold Time (Using Product Term Gate) | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{GO}$ | Latch Gate to Output | | 11 | | 12 | | 13 | | 14 | ns |

## BASIC (all signals from within PAL block except global control signals) (Continued)

| Parameter Symbol | Parameter Description | -10 | | -12 | | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{GOL}$ | Latch (Input or Output) Gate to Output through Transparent Latch | | 18 | | 19 | | 20 | | 21 | ns |
| $t_{GCO}$ | Latch Gate to Combinatorial Output | | 18 | | 19 | | 20 | | 21 | ns |
| $t_{IGS}$ | Latch Gate to Output Latch Setup | 11 | | 12 | | 13 | | 14 | | ns |
| $t_{GW}$ | Gate Width LOW (for LOW Transparent) or High (for HIGH Transparent) | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{BUF}$ | Delay Savings for Using Internal Feedback Instead of Pin Feedback (I/Os Only, No Savings for Buried) | 0.5 | 2 | 0.5 | 2 | 0.5 | 2 | 0.5 | 2 | ns |

## ASYNCHRONOUS SET AND RESET, OUTPUT ENABLE, CLOCK ENABLE

| Parameter Symbol | Parameter Description | -10 | | -12 | | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RP}$ | Asynchronous Reset or Preset to Registered or Latched Output | | 12 | | 14 | | 16 | | 18 | ns |
| $t_{PRW}$ | Asynchronous Reset or Preset Width | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{PRR}$ | Asynchronous Reset or Preset Recovery Time | 8 | | 9 | | 10 | | 11 | | ns |
| $t_{EA}$ | Input, I/O, or Feedback to Output Enable | | 10 | | 12 | | 15 | | 20 | ns |
| $t_{ER}$ | Input, I/O, or Feedback to Output Disable | | 10 | | 12 | | 15 | | 20 | ns |
| $t_{CES}$ | Setup Time from Clock Enable to Next Clock Pulse | 6 | | 7 | | 7 | | 8 | | ns |
| $t_{CEH}$ | Hold Time for Clock Enable After Last Enabled Clock Pulse | 5 | | 6 | | 6 | | 7 | | ns |
| $t_{RCEH}$ | Hold Time for Registered Clock Enable After Last Enabled Clock Pulse | 0 | | 0 | | 0 | | 0 | | ns |

## REGISTERS and LATCHES (input and output, BLOCK level)

| Parameter Symbol | Parameter Description | -10 | | -12 | | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PDIL}$ | Input, I/O, or Feedback to Output Through Transparent Input Latch | | 15 | | 17 | | 20 | | 21 | ns |
| $t_{ICOG}$ | Input Register Global Clock to Combinatorial Output | | 14 | | 16 | | 18 | | 20 | ns |
| $t_{ICOA}$ | Input Register Product Term Clock to Combinatorial Output | | 18 | | 19 | | 20 | | 21 | ns |
| $t_{SIRS}$ | Input Register Setup Time Using Global Clock | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{SIRA}$ | Input Register Setup Time Using Product Term Clock | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HIRS}$ | Input Register Hold Time Using Global Clock | 4 | | 4 | | 4 | | 4 | | ns |
| $t_{HIRA}$ | Input Register Hold Time Using Product Term Clock | 7 | | 7 | | 7 | | 7 | | ns |
| $t_{WICW}$ | Input Register Clock Width Low or High | 5 | | 6 | | 7 | | 8 | | ns |
| $f_{MAXI}$ | Maximum Input Register Frequency | 100 | | 83.3 | | 71.4 | | 62.5 | | MHz |
| $t_{RCSS}$ | Register Using Global Clock to Output Register Using Global Clock Setup Time | 10 | | 12 | | 15 | | 20 | | ns |
| $t_{RCSA}$ | Register Using Global Clock to Output Register Using Product Term Clock Setup Time | 15 | | 17 | | 18 | | 20 | | ns |
| $t_{RCAS}$ | Register Using Product Term Clock to Output Register Using Global Clock Setup Time | 15 | | 17 | | 18 | | 20 | | ns |
| $t_{RCAA}$ | Register Using Product Term Clock to Output Register Using Same Product Term Clock Setup Time | 10 | | 12 | | 15 | | 20 | | ns |
| $t_{SIL}$ | Input Latch Setup Time | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{HIL}$ | Input Latch Hold Time | 7 | | 7 | | 7 | | 7 | | ns |
| $t_{SLL}$ | Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate | 10 | | 11 | | 12 | | 13 | | ns |
| $t_{PDLL}$ | Input, I/O, or Feedback to Output Through Transparent Input and Output Latches | | 16 | | 18 | | 20 | | 22 | ns |

## INTERCONNECT

| Parameter Symbol | Parameter Description | -10 | | -12 | | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{BLK}$ | Interconnect delay between blocks. If a signal depends on inputs not in the same block, but in the same segment, this delay must be added to $t_{PD}$, $t_{SS}$, $t_{SA}$, $t_{COA}$, $t_{SL}$, $t_{GO}$, $t_{GOL}$, $t_{GCO}$, $t_{IGS}$, $t_{RP}$, $t_{EA}$, $t_{ER}$, $t_{CES}$, $t_{PDL}$, $t_{ICO}$, $t_{RCSS}$, $t_{RCAS}$, $t_{RCAA}$, $t_{PDLL}$, $t_{SLL}$. | | 2.0 | | 2.0 | | 2.0 | | 2.0 | ns |
| $t_{SEG}$ | Interconnect delay between segments. This parameter includes all block interconnect delay. If a signal depends on inputs not in the same segment, this delay must be added to $t_{PD}$, $t_{SS}$, $t_{SA}$, $t_{COA}$, $t_{SL}$, $t_{GO}$, $t_{GOL}$, $t_{GCO}$, $t_{IGS}$, $t_{RP}$, $t_{EA}$, $t_{ER}$, $t_{CES}$, $t_{PDL}$, $t_{ICO}$, $t_{RCSS}$, $t_{RCAS}$, $t_{RCAA}$, $t_{PDLL}$, $t_{SLL}$. | | 6 | | 6 | | 6 | | 6 | ns |

## POWER, LOGIC, AND SLEW (Please see individual device data sheets for details.)

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies (Fmax/2).*

## ABSOLUTE MAXIMUM RATINGS

### MACH 5 LV IND -10, -12, -15, -20

Storage Temperature . . . . . –65°C to +150°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . 0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (0°C to +70°C) . . . . . 200 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Ambient Temperature ($T_A$)
Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage ($V_{CC}$)
with Respect to Ground . . . . . +3.0 V to +3.6 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## 3.3-V DC CHARACTERISTICS over INDUSTRIAL operating ranges

| Parameter Symbol | Parameter Description | Test Description | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –100 µA | $V_{CC}$ –0.2 | | V |
| | | | $I_{OH}$ = 3.2 mA | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 100 µA | | | V |
| | | | $I_{OH}$ = 16 mA (Note 1) | | | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 2) | | 2.0 | 5.5 | V |
| $V_{IL}$ | Input LOW Voltage | $V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 2) | | –0.3 | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 3.6, $V_{CC}$ = Max (Note 3) | | | 5 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0, $V_{CC}$ = Max (Note 3) | | | –5 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 3.6, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | | 5 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | | –5 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 3) | | –15 | –160 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ or $I_{IH}$ and $I_{OZH}$.*
3. *Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | I/CLK pin | $V_{IN}$ = 2.0 V | 3.3 V, 25°C, 1 MHz | 12 | pF |
| $C_{I/O}$ | I/O pin | $V_{OUT}$ = 2.0 V | 3.3 V, 25°C, 1 MHz | 10 | pF |

***Note:***

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

## SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

### BASIC (all signals from within PAL block except global control signals)

| Parameter Symbol | Parameter Description | -10 | | -12 | | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PD}$ | Input, I/O, or Feedback to Combinatorial Output or Input, I/O, or Feedback to Output through Transparent Output Latch | 2 | 10 | 2 | 12 | 2 | 15 | 2 | 20 | ns |
| $t_{SS}$ | Setup Time from Input, I/O, or Feedback to Global Clock | 5 | | 6 | | 8 | | 10 | | ns |
| $t_{HS}$ | Register Data Hold Time Using a Global Clock | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{COS}$ | Global Clock to Output (Pin Clock) | | 7 | | 8 | | 10 | | 12 | ns |
| $t_{WLS}$ | Global Clock Low Width (Note 3) | 4 | | 5 | | 6 | | 7 | | ns |
| $t_{WHS}$ | Global Clock High Width (Note 3) | 4 | | 5 | | 6 | | 7 | | ns |
| $f_{MAX}$ | External Feedback, PAL Block Level $1/(t_{SS} + t_{COS})$ | 83 | | 71 | | 55 | | 45.5 | | MHz |
| | Internal Feedback PAL Block Level | 100 | | 83.3 | | 83.3 | | 71.4 | | MHz |
| | No Feedback PAL Block Level | 125 | | 100 | | 83.3 | | 71.4 | | MHz |
| $t_{SA}$ | Setup Time from Input, I/O, or Feedback to Product Term Clock, PAL Block Level | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{HA}$ | Output Register Data Hold Time Using a Product Term Clock | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{COA}$ | Product Term Clock to Output | | 12 | | 15 | | 17 | | 20 | ns |
| $t_{WLA}$ | Product Term Clock Width LOW | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{WHA}$ | Product Term Clock Width HIGH | 5 | | 6 | | 7 | | 8 | | ns |
| $f_{MAXA}$ | External Feedback, PAL Block Level $1/(t_{SA} + t_{COA})$ | 58 | | 47.6 | | 42 | | 35 | | MHz |
| | Internal Feedback, PAL Block Level | 72 | | 60 | | 52 | | 45 | | MHz |
| | No Feedback, PAL Block Level | 100 | | 83.3 | | 71.4 | | 62.5 | | MHz |
| $t_{SL}$ | Setup Time from Input, I/O, or Feedback to Product Term Gate | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{HL}$ | Latch Data Hold Time (Using Product Term Gate) | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{GO}$ | Latch Gate to Output | | 11 | | 12 | | 13 | | 14 | ns |

## BASIC (all signals from within PAL block except global control signals) (Continued)

| Parameter Symbol | Parameter Description | -10 | | -12 | | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{GOL}$ | Latch Gate to Output through Transparent Latch | | 18 | | 19 | | 20 | | 21 | ns |
| $t_{GCO}$ | Latch Gate to Combinatorial Output | | 18 | | 19 | | 20 | | 21 | ns |
| $t_{IGS}$ | Latch Gate to Output Latch Setup | 11 | | 12 | | 13 | | 14 | | ns |
| $t_{GW}$ | Gate Width LOW (for LOW Transparent) or High (for HIGH Transparent) | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{BUF}$ | Delay Savings for Using Internal Feedback Instead of Pin Feedback (I/Os Only, No Savings for Buried) | 0.5 | 2 | 0.5 | 2 | 0.5 | 2 | 0.5 | 2 | ns |

## ASYNCHRONOUS SET and RESET, OUTPUT ENABLE, CLOCK ENABLE

| Parameter Symbol | Parameter Description | -10 | | -12 | | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RP}$ | Asynchronous Reset or Preset to Registered or Latched Output | | 12 | | 14 | | 16 | | 18 | ns |
| $t_{PRW}$ | Asynchronous Reset or Preset Width | 5 | | 6 | | 7 | | 8 | | ns |
| $t_{PRR}$ | Asynchronous Reset or Preset Recovery Time | 8 | | 9 | | 10 | | 11 | | ns |
| $t_{EA}$ | Input, I/O, or Feedback to Output Enable | 2 | 10 | 2 | 12 | 2 | 15 | 2 | 20 | ns |
| $t_{ER}$ | Input, I/O, or Feedback to Output Disable | | 10 | | 12 | | 15 | | 20 | ns |
| $t_{CES}$ | Setup Time from Clock Enable to Next Clock Pulse | 6 | | 7 | | 7 | | 8 | | ns |
| $t_{CEH}$ | Hold Time for Clock Enable Following Last Enabled Clock Pulse | 5 | | 6 | | 6 | | 7 | | ns |
| $t_{RCEH}$ | Hold Time for Registered Clock Enable After Last Enabled Clock Edge | 0 | | 0 | | 0 | | 0 | | ns |

## REGISTERS and LATCHES (input and output, BLOCK level)

| Parameter Symbol | Parameter Description | -10 | | -12 | | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PDIL}$ | Input, I/O, or Feedback to Output Through Transparent Input Latch | | 15 | | 17 | | 20 | | 21 | ns |
| $t_{ICOG}$ | Input Register Global Clock to Combinatorial Output | | 14 | | 16 | | 18 | | 20 | ns |
| $t_{ICOA}$ | Input Register Product Term Clock to Combinatorial Output | | 18 | | 19 | | 20 | | 21 | ns |
| $t_{SIRS}$ | Input Register Setup Time Using Global Clock | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{SIRA}$ | Input Register Setup Time Using Product Term Clock | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HIRS}$ | Input Register Hold Time Using Global Clock | 4 | | 4 | | 4 | | 4 | | ns |
| $t_{HIRA}$ | Input Register Hold Time Using Product Term Clock | 7 | | 7 | | 7 | | 7 | | ns |
| $t_{WICW}$ | Input Register Clock Width Low or High | 5 | | 6 | | 7 | | 8 | | ns |
| $f_{MAXI}$ | Maximum Input Register Frequency | 100 | | 83.3 | | 71.4 | | 62.5 | | MHz |
| $t_{RCSS}$ | Register Using Global Clock to Output Register Using Global Clock Setup Time | 10 | | 12 | | 15 | | 20 | | ns |
| $t_{RCSA}$ | Register Using Global Clock to Output Register Using Product Term Clock Setup Time | 15 | | 17 | | 18 | | 20 | | ns |
| $t_{RCAS}$ | Register Using Product Term Clock to Output Register Using Global Clock Setup Time | 15 | | 17 | | 18 | | 20 | | ns |
| $t_{RCAA}$ | Register Using Product Term Clock to Output Register Using Same Product Term Clock Setup Time | 10 | | 12 | | 15 | | 20 | | ns |
| $t_{SIL}$ | Input Latch Setup Time | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{HIL}$ | Input Latch Hold Time | 7 | | 7 | | 7 | | 7 | | ns |
| $t_{SLL}$ | Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate | 10 | | 11 | | 12 | | 13 | | ns |

## INTERCONNECT

| Parameter Symbol | Parameter Description | -10 | | -12 | | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{BLK}$ | Interconnect delay between blocks. If a signal depends on inputs not in the same block, but in the same segment, this delay must be added to $t_{PD}$, $t_{SS}$, $t_{SA}$, $t_{COA}$, $t_{SL}$, $t_{GO}$, $t_{GOL}$, $t_{GCO}$, $t_{IGS}$, $t_{RP}$, $t_{EA}$, $t_{ER}$, $t_{CES}$, $t_{PDL}$, $t_{ICO}$, $t_{RCSS}$, $t_{RCAS}$, $t_{RCAA}$, $t_{PDLL}$, $t_{SLL}$. | | 2.0 | | 2.0 | | 2.0 | | 2.0 | ns |
| $t_{SEG}$ | Interconnect delay between segments. This parameter includes all block interconnect delay. If a signal depends on inputs not in the same segment, this delay must be added to $t_{PD}$, $t_{SS}$, $t_{SA}$, $t_{COA}$, $t_{SL}$, $t_{GO}$, $t_{GOL}$, $t_{GCO}$, $t_{IGS}$, $t_{RP}$, $t_{EA}$, $t_{ER}$, $t_{CES}$, $t_{PDL}$, $t_{ICO}$, $t_{RCSS}$, $t_{RCAS}$, $t_{RCAA}$, $t_{PDLL}$, $t_{SLL}$. | | 6 | | 6 | | 6 | | 6 | ns |

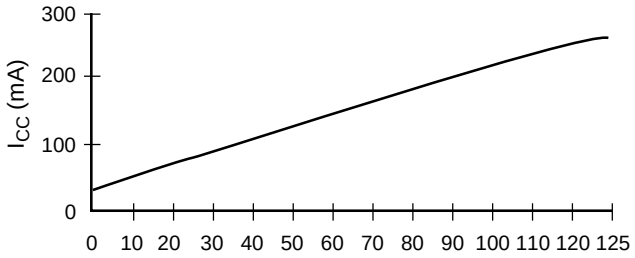
## POWER, LOGIC, AND SLEW (Please see individual device data sheets for details.)

***Notes:***

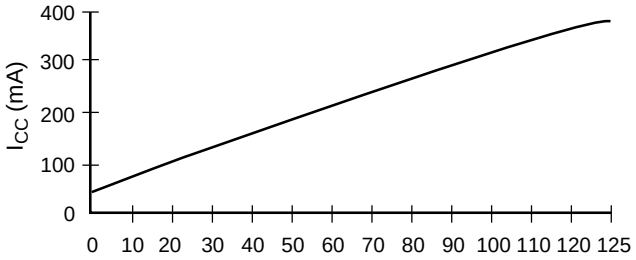
2. *See Switching Test Circuit for test conditions.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies (Fmax/2).*

## $I_{CC}$ vs. FREQUENCY

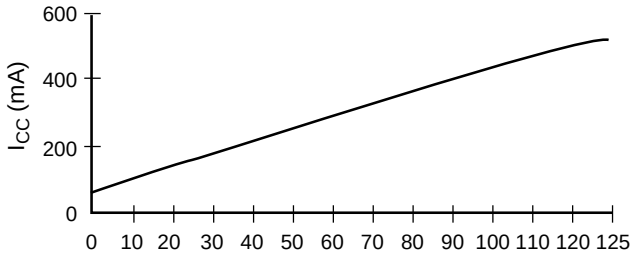
These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power.



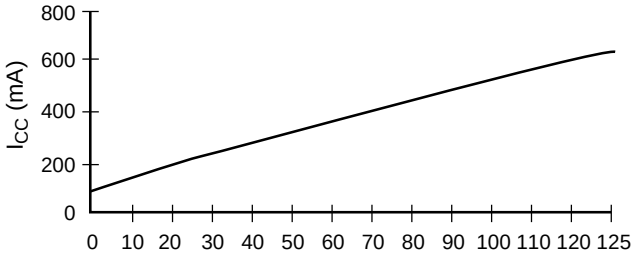

M5-128/M5LV-128



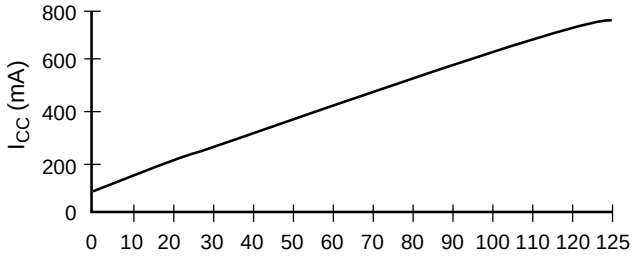

M5-192/M5LV-192



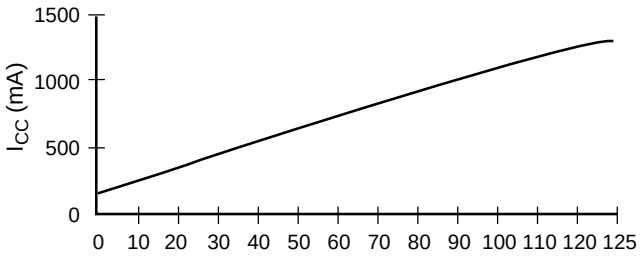

M5-256/M5LV-256




M5-320/M5LV-320



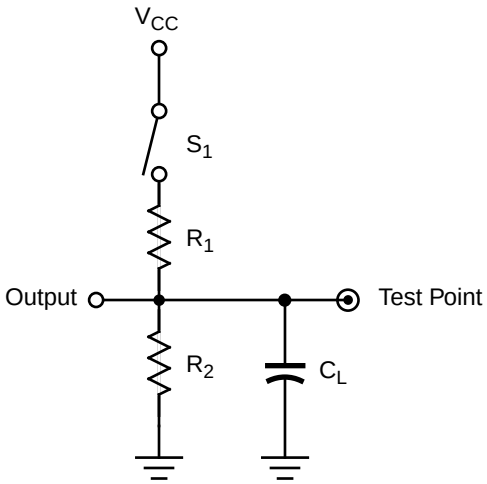

M5-384/M5LV-384




M5-512/M5LV-512

20446D-16

## SWITCHING TEST CIRCUIT




20446D-17

| Specification | $S_1$ | $C_L$ | Commercial | | Measured Output Value |
|---|---|---|---|---|---|
| | | | $R_1$ | $R_2$ | |
| $t_{PD}$, $t_{CO}$ | Closed | 35 pF (30 pF) | 300 Ω (1.6 KΩ) | 390 Ω (1.6 KΩ) | 1.5 V |
| $t_{EA}$ | Z → H: Open<br>Z → L: Closed | | | | |
| $t_{ER}$ | H → Z: Open<br>L → Z: Closed | 5 pF | | | H → Z: $V_{OH}$ – 0.5 V<br>L → Z: $V_{OL}$ + 0.5 V |

* *Switching several outputs simultaneously should be avoided for accurate measurement.*

*Values in parentheses are for 3.3-V devices.*

## $f_{MAX}$ PARAMETERS

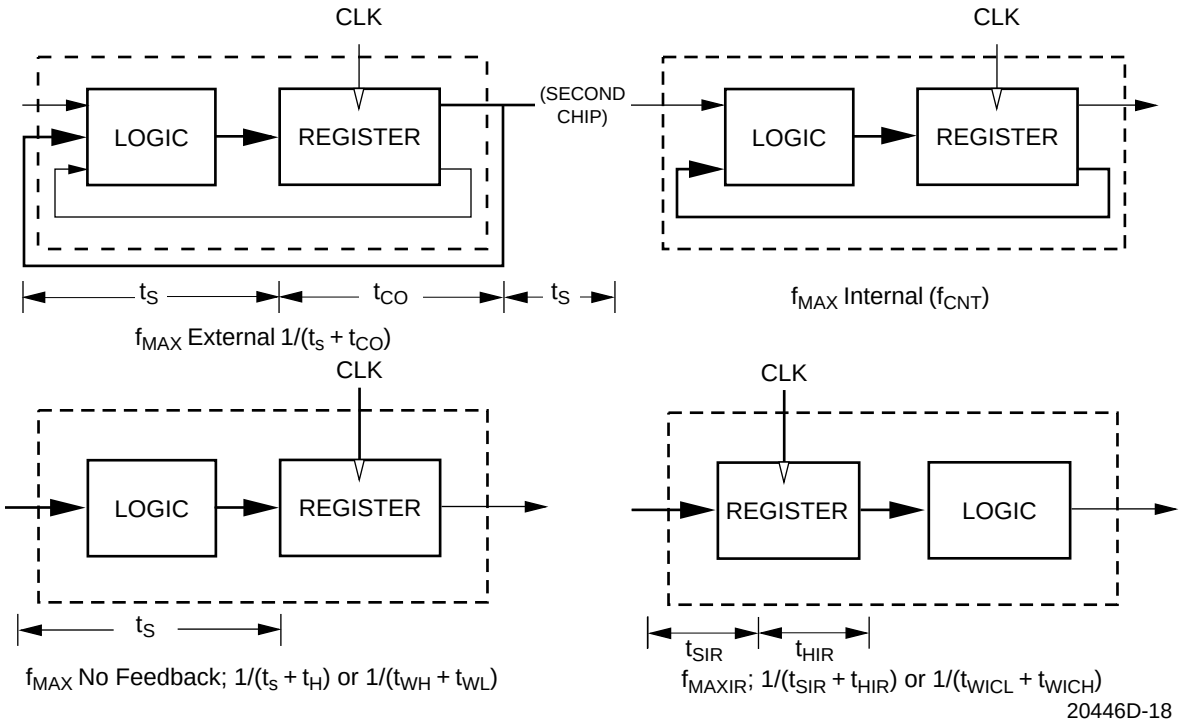
The parameter $f_{MAX}$ is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, $f_{MAX}$ is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, $f_{MAX}$, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This $f_{MAX}$ is designated "$f_{MAX}$ external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This $f_{MAX}$ is designated "$f_{MAX}$ internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "$f_{CNT.}$"

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each $f_{MAX}$ type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third $f_{MAX}$, designated "$f_{MAX}$ no feedback."

For devices with input registers, one additional $f_{MAX}$ parameter is specified: $f_{MAXIR}$. Because this involves no feedback, it is calculated the same way as $f_{MAX}$ no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that $f_{MAXIR}$ is specified as $1/(t_{WICL} + t_{WICH})$. Note that if both input and output registers are used in the same path, the overall frequency will be limited by $t_{ICS}$. All frequencies except $f_{MAX}$ internal are calculated from other measured AC parameters. $f_{MAX}$ internal is measured directly.



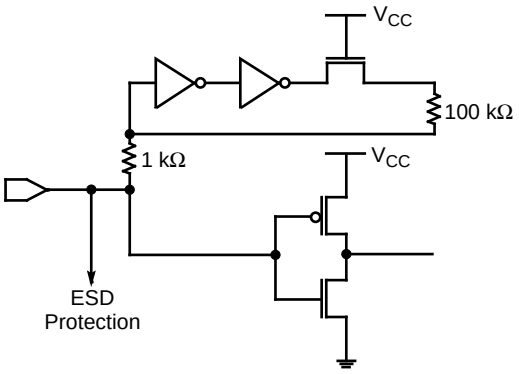
## ENDURANCE CHARACTERISTICS

The MACH families are manufactured using Vantis' advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

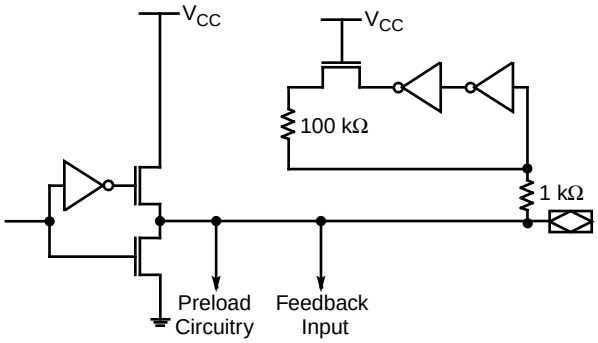
### Endurance Characteristics

| Parameter Symbol | Parameter Description | | Units | Test Conditions |
|---|---|---|---|---|
| $t_{DR}$ | Min Pattern Data Retention Time | 10 | Years | Max Storage Temperature |
| | | 20 | Years | Max Operating Temperature |
| N | Max Reprogramming Cycles | 100 | Cycles | Normal Programming Conditions |

## INPUT/OUTPUT EQUIVALENT SCHEMATICS




**Input**




**I/O**

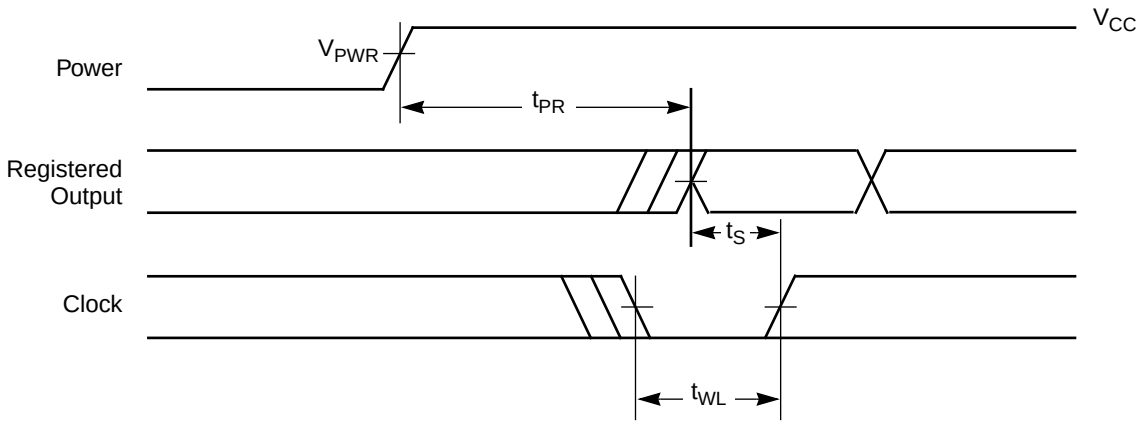
20446D-19

## POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways $V_{CC}$ can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The $V_{CC}$ rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

| Parameter Symbol | Parameter Descriptions | Max | Unit |
|---|---|---|---|
| $t_{PR}$ | Power-Up Reset Time | 10 | µs |
| $t_S$ | Input or Feedback Setup Time | See Switching Characteristics | |
| $t_{WL}$ | Clock Width LOW | | |




20446D-20

**Power-Up Reset Waveform**

*$V_{PWR}$ = 4 V for 5-V devices and 2.7 for 3.3-V devices.*

## DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the local Vantis sales office.

| MANUFACTURER | SOFTWARE DEVELOPMENT SYSTEMS |
|---|---|
| Vantis Corporation<br>P.O. Box 3755<br>920 DeGuigne Drive<br>Sunnyvale, CA 94088<br>(408) 732-0555 or 1(888) 826-8472 (VANTIS2)<br>http://www.vantis.com | MACHXL Software<br>Vantis-ABEL Software<br>Vantis-Synario Software |
| Aldec, Inc.<br>3 Sunset Way, Suite F<br>Henderson, NV 89014<br>(702) 456-1222 or (800) 487-8743 | ACTIVE-CAD |
| Cadence Design Systems<br>555 River Oaks Pkwy<br>San Jose, CA 95134<br>(408) 943-1234 or (800) 746-6223 | PIC Designer<br>Concept/Composer<br>Synergy<br>Leapfrog/Verilog-XL |
| Exemplar Logic, Inc.<br>815 Atlantic Avenue, Suite 105<br>Alameda, CA 94501<br>(510) 337-3700 | Leonardo™<br>Galileo™ |
| Logic Modeling<br>19500 NW Gibbs Dr.<br>P.O. Box 310<br>Beaverton, OR 97075<br>(800) 346-6335 | SmartModel® Library |
| Mentor Graphics Corp.<br>8005 S.W. Boeckman Rd.<br>Wilsonville, OR 97070-7777<br>(800) 547-3000 or (503) 685-7000 | Design Architect, PLDSynthesis™ II<br>Autologic II Synthesizer, QuickSim Simulator, QuickHDL Simulator |
| MicroSim Corp.<br>20 Fairbanks<br>Irvine, CA 92718<br>(714) 770-3022 | MicroSim Design Lab<br>PLogic, PLSyn |
| MINC Inc.<br>6755 Earl Drive, Suite 200<br>Colorado Springs, CO 80918<br>(800) 755-FPGA or (719) 590-1155 | PLDesigner-XL™ Software |
| Model Technology<br>8905 S.W. Nimbus Avenue, Suite 150<br>Beaverton, OR 97008<br>(503) 641-1340 | V-System/VHDL |
| OrCAD, Inc.<br>9300 S.W. Nimbus Avenue<br>Beaverton, OR 97008<br>(503) 671-9500 or (800) 671-9505 | OrCAD Express |
| Synario® Design Automation<br>10525 Willows Road N.E.<br>P.O. Box 97046<br>Redmond, WA 98073-9746<br>(800) 332-8246 or (206) 881-6444 | ABEL™<br>Synario™ Software |

| MANUFACTURER | SOFTWARE DEVELOPMENT SYSTEMS |
|---|---|
| Synopsys<br>700 E. Middlefield Rd.<br>Mountain View, CA 94040<br>(415) 962-5000 or (800) 388-9125 | FPGA or Design Compiler<br>(Requires MINC PLDesigner-XL™)<br>VSS Simulator |
| Synplicity, Inc.<br>624 East Evelyn Ave.<br>Sunnyvale, CA 94086<br>(408) 617-6000 | Synplify |
| Teradyne EDA<br>321 Harrison Ave.<br>Boston, MA 02118<br>(800) 777-2432 or (617) 422-2793 | MultiSIM Interactive Simulator<br>LASAR |
| VeriBest, Inc.<br>6101 Lookout Road, Suite A<br>Boulder, CO 80301<br>(800) 837-4237 | VeriBest PLD |
| Viewlogic Systems, Inc.<br>293 Boston Post Road West<br>Marlboro, MA 01752<br>(800) 873-8439 or (508) 480-0881 | Viewdraw, ViewPLD, Viewsynthesis<br>Speedwave Simulator, ViewSim Simulator, VCS Simulator |
| **MANUFACTURER** | **TEST GENERATION SYSTEM** |
| Acugen Software, Inc.<br>427-3 Amherst St., Suite 391<br>Nashua, NH 03063<br>(603) 881-8821 | ATGEN™ Test Generation Software |
| iNt GmbH<br>Busenstrasse 6<br>D-8033 Martinsried, Munich, Germany<br>(87) 857-6667 | PLDCheck 90 |

*Vantis is not responsible for any information relating to the products of third parties. The inclusion of such information is not a representation nor an endorsement by Vantis of these products.*

## APPROVED PROGRAMMERS (subject to change)

For more information on the products listed below, please consult the local Vantis sales office.

| MANUFACTURER | PROGRAMMER CONFIGURATION |
|---|---|
| Advin Systems, Inc.<br>1050-L East Duane Ave.<br>Sunnyvale, CA 940 86<br>(408) 243-7000 or (800) 627-2456<br>BBS (408) 737-9200<br>Fax (408) 736-2503 | Pilot-U40 Pilot-U84 MVP |
| BP Microsystems<br>1000 N. Post Oak Rd., Suite 225<br>Houston, TX 77055-7237<br>(800) 225-2102 or (713) 688-4600<br>BBS (713) 688-9283<br>Fax (713) 688-0920 | BP1200 BP1400 BP2100 BP2200 |
| Data I/O Corporation<br>10525 Willows Road N.E.<br>P.O. Box 97046<br>Redmond, WA 98073-9746<br>(800) 426-1045 or (206) 881-6444<br>BBS (206) 882-3211<br>Fax (206) 882-1043 | UniSite™ Model 2900 Model 3900 AutoSite |
| Hi-Lo Systems<br>4F, No. 2, Sec. 5, Ming Shoh E. Road<br>Taipei, Taiwan<br>(886) 2-764-0215<br>Fax (886) 2-756-6403<br>or<br>Tribal Microsystems / Hi-Lo Systems<br>44388 South Grimmer Blvd.<br>Fremont, CA 94538<br>(510) 623-8859<br>BBS (510) 623-0430<br>Fax (510) 623-9925 | ALL-07 FLEX-700 |
| SMS GmbH<br>Im Grund 15<br>88239 Wangen<br>Germany<br>(49) 7522-97280<br>Fax (49) 7522-972850<br>or<br>SMS USA<br>544 Weddell Dr. Suite 12<br>Sunnyvale, CA 94089<br>(408) 542-0388 | Sprint Expert Sprint Optima Multisite |
| Stag House<br>Silver Court Watchmead, Welwyn Garden City<br>Herfordshire UK AL7 1LT<br>44-1-707-332148<br>Fax 44-1-707-371503 | Stag Quazar |

| MANUFACTURER | PROGRAMMER CONFIGURATION |
|---|---|
| System General<br>1603A South Main Street<br>Milpitas, CA 95035<br>(408) 263-6667<br>BBS (408) 262-6438<br>Fax (408) 262-9220<br>or<br>3F, No. 1, Alley 8, Lane 45<br>Bao Shing Road, Shin Diau<br>Taipei, Taiwan<br>(886) 2-917-3005<br>Fax (886) 2-911-1283 | Turpro-1 Turpro-1/FX Turpro-1/TX |

## APPROVED ADAPTER MANUFACTURERS

| MANUFACTURER | PROGRAMMER CONFIGURATION |
|---|---|
| California Integration Coordinators, Inc.<br>656 Main Street<br>Placerville, CA 95667<br>(916) 626-6168<br>Fax (916) 626-7740 | MACH/PAL Programming Adapters |
| Emulation Technology, Inc.<br>2344 Walsh Ave., Bldg. F<br>Santa Clara, CA 95051<br>(408) 982-0660<br>Fax (408) 982-0664 | Adapt-A-Socket®<br>Programming Adapters |

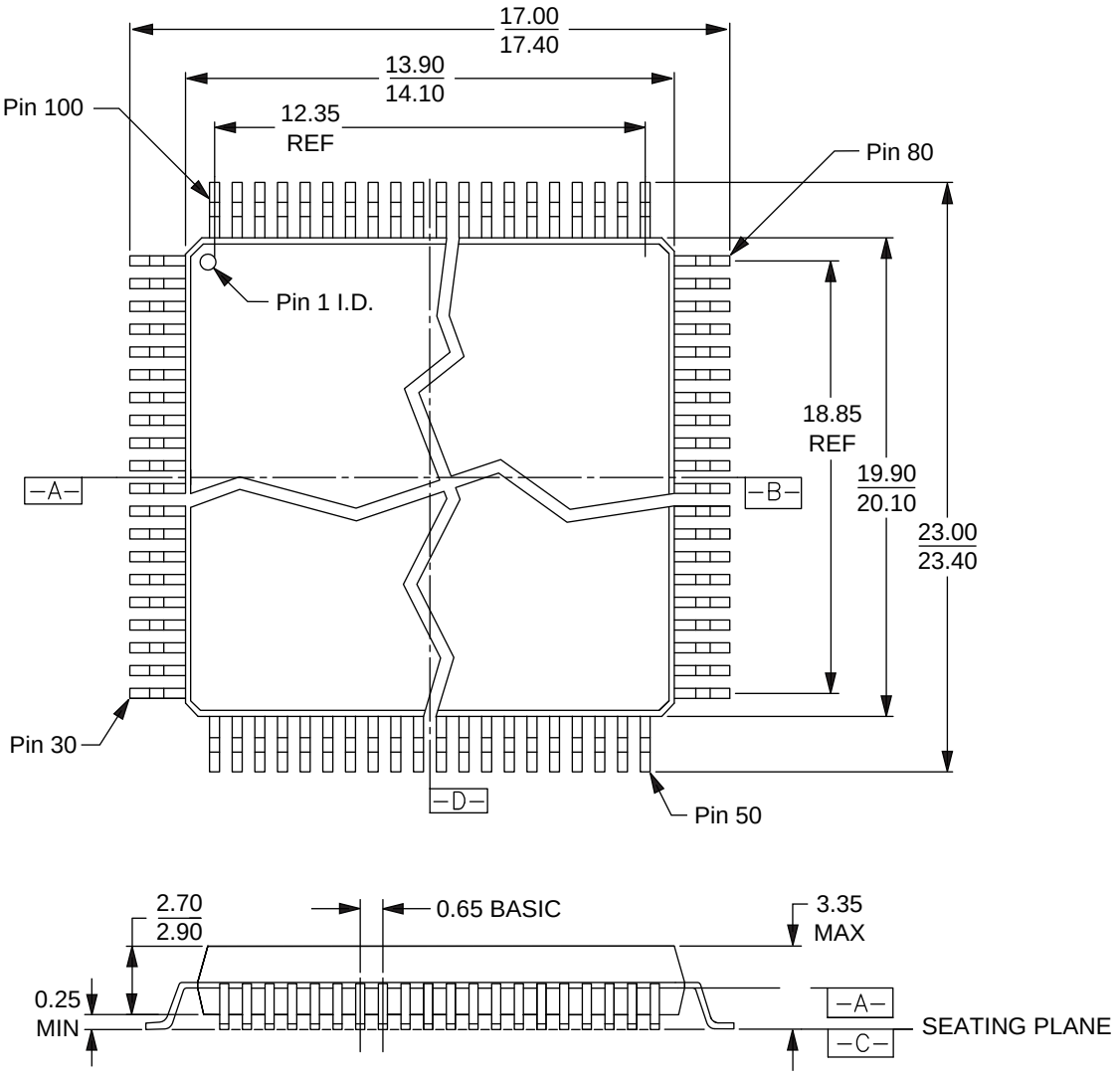
## APPROVED ON-BOARD ISP PROGRAMMING TOOLS

| MANUFACTURER | PROGRAMMER CONFIGURATION |
|---|---|
| Corelis, Inc.<br>12607 Hidden Creek Way, Suite H<br>Cerritos, California 70703<br>(310) 926-6727 | JTAGPROG™ |
| Vantis Corporation<br>P.O. Box 3755<br>920 DeGuigne Drive<br>Sunnyvale, CA 94088<br>(408) 732-0555 or 1(888) 826-8472 (VANTIS2)<br>http://www.vantis.com | MACHPRO® |

# PHYSICAL DIMENSIONS

## PQR100

### 100-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)

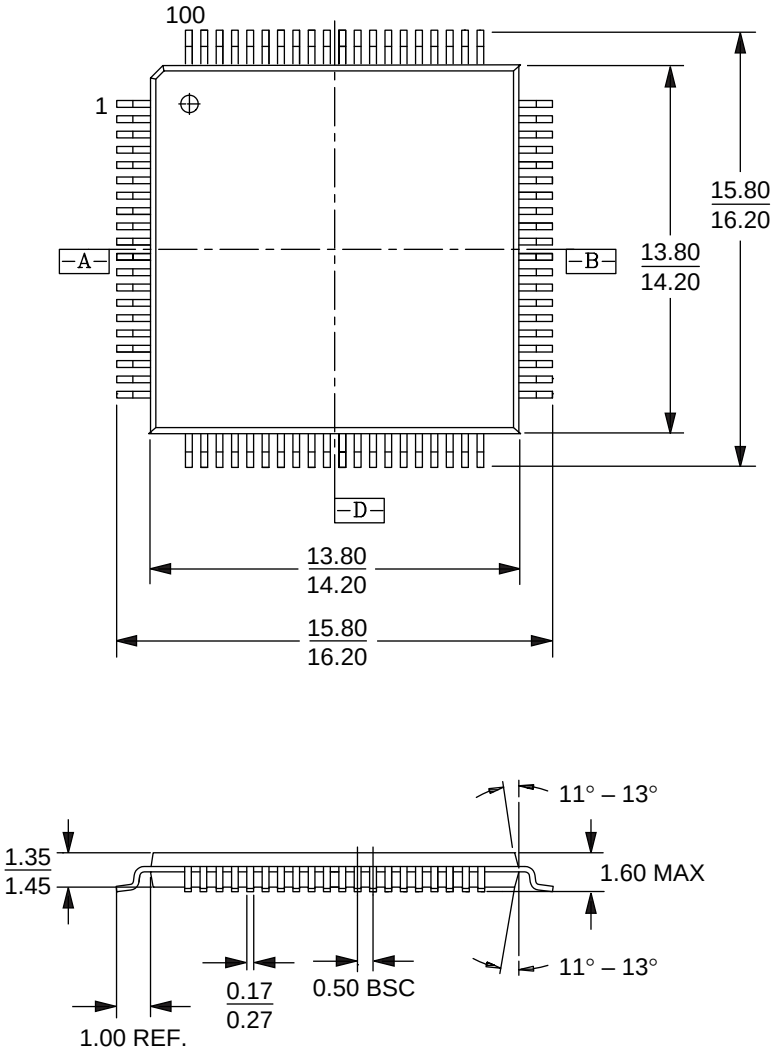



16-038-PQR-1_AH
PQR100
DP92
6-20-96 lv

# PHYSICAL DIMENSIONS

## PQL100

### 100-Pin Thin Quad Flat Pack; Trimmed and Formed (measured in millimeters)

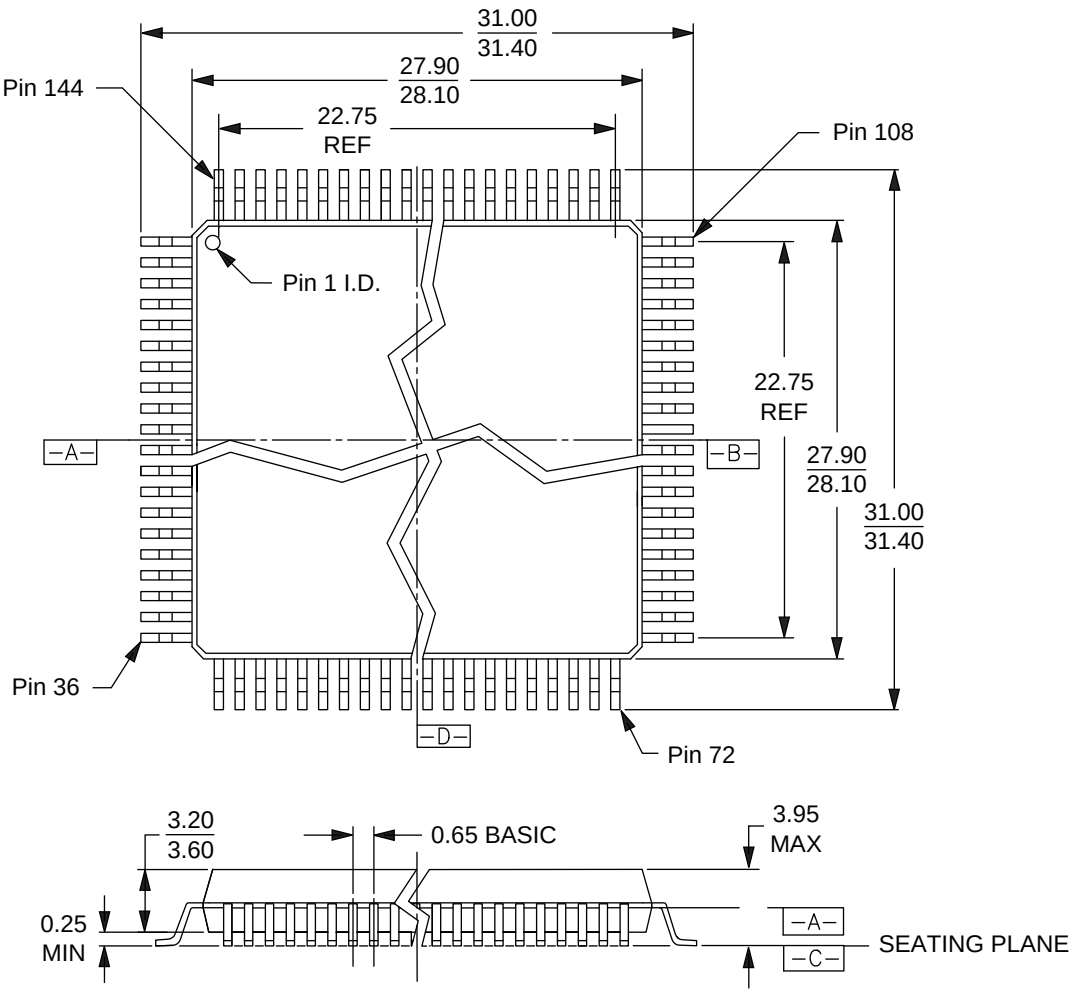



16-038-PQT-2_AI
PQL100
9.3.96 lv

# PHYSICAL DIMENSIONS

## PQR144

### 144-Pin Thin Quad Flat Pack; Trimmed and Formed (measured in millimeters)

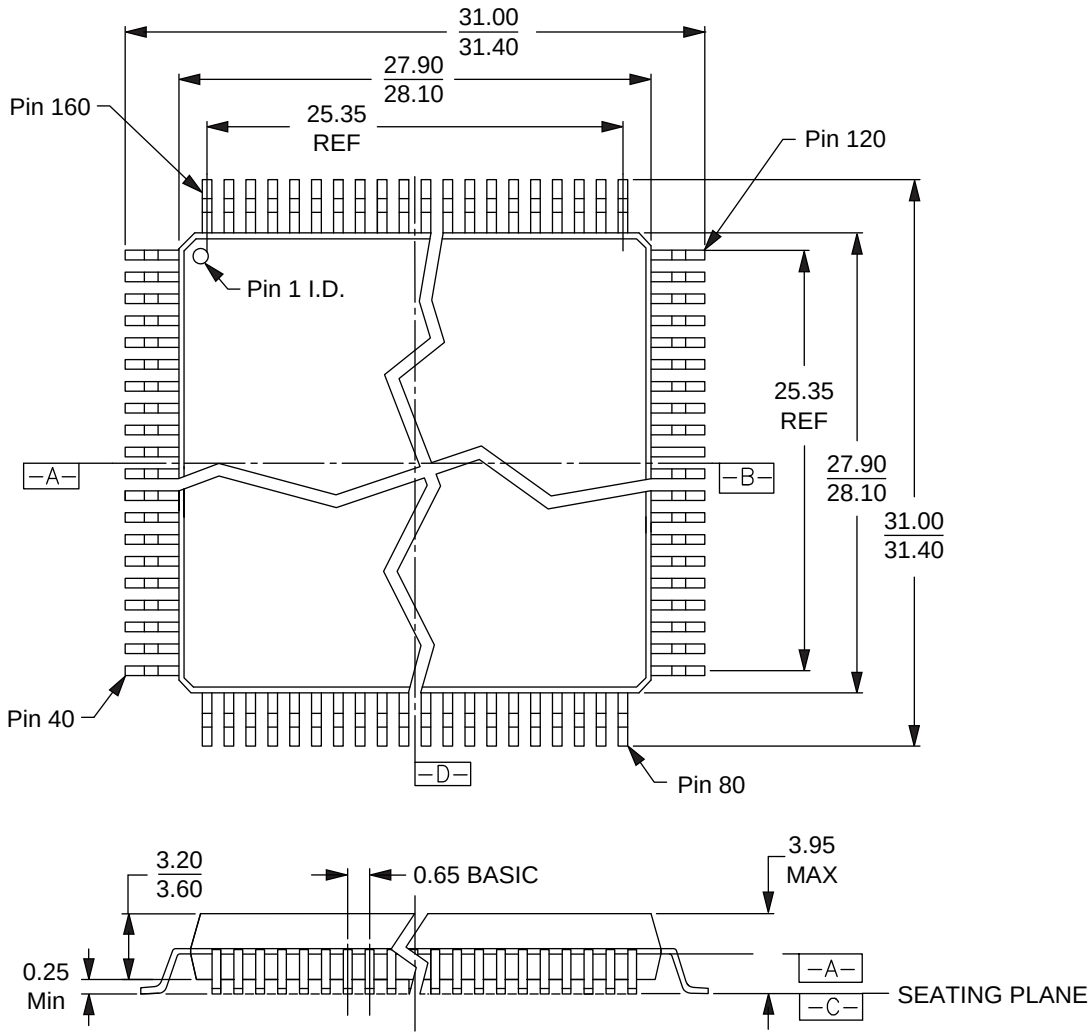



16-038-PQR-1_AH
PQR144
EC95

# PHYSICAL DIMENSIONS

## PQR160

### 160-Pin Thin Quad Flat Pack; Trimmed and Formed (measured in millimeters)

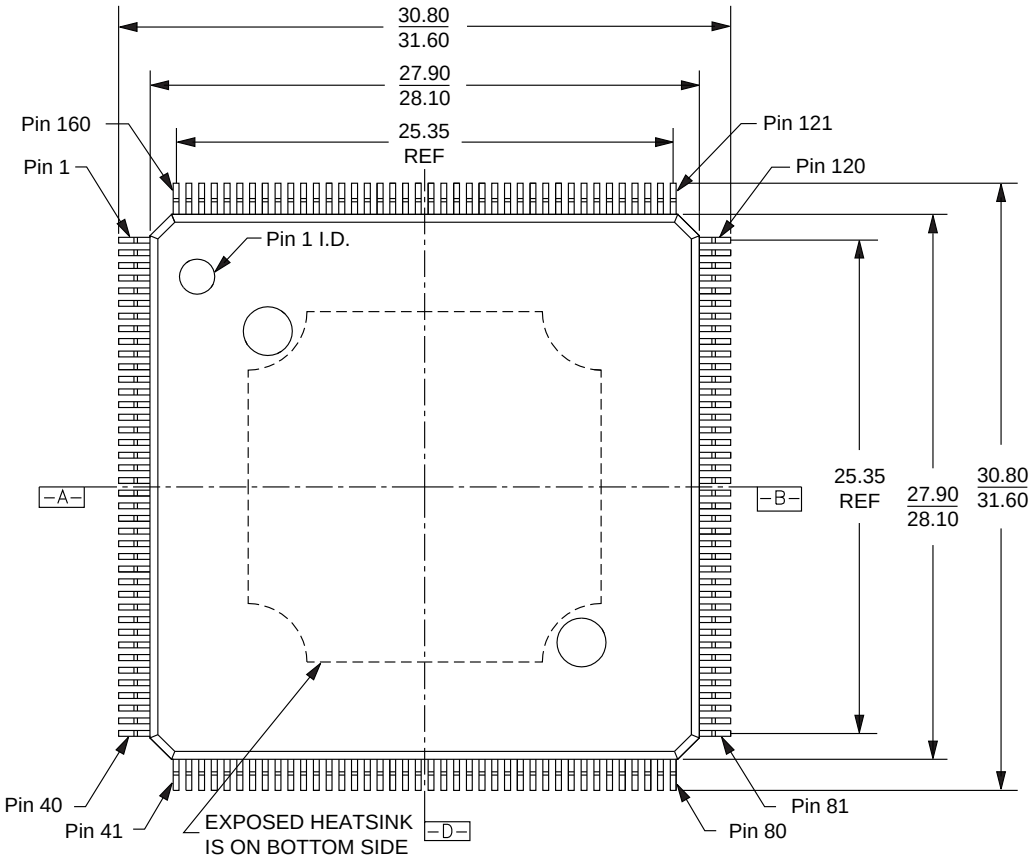



16-038-PQR-1
PQR160
12-22-95 lv

# PHYSICAL DIMENSIONS

## PQE160

### 160-Pin Thin Quad Flat Pack; Trimmed and Formed (measured in millimeters)

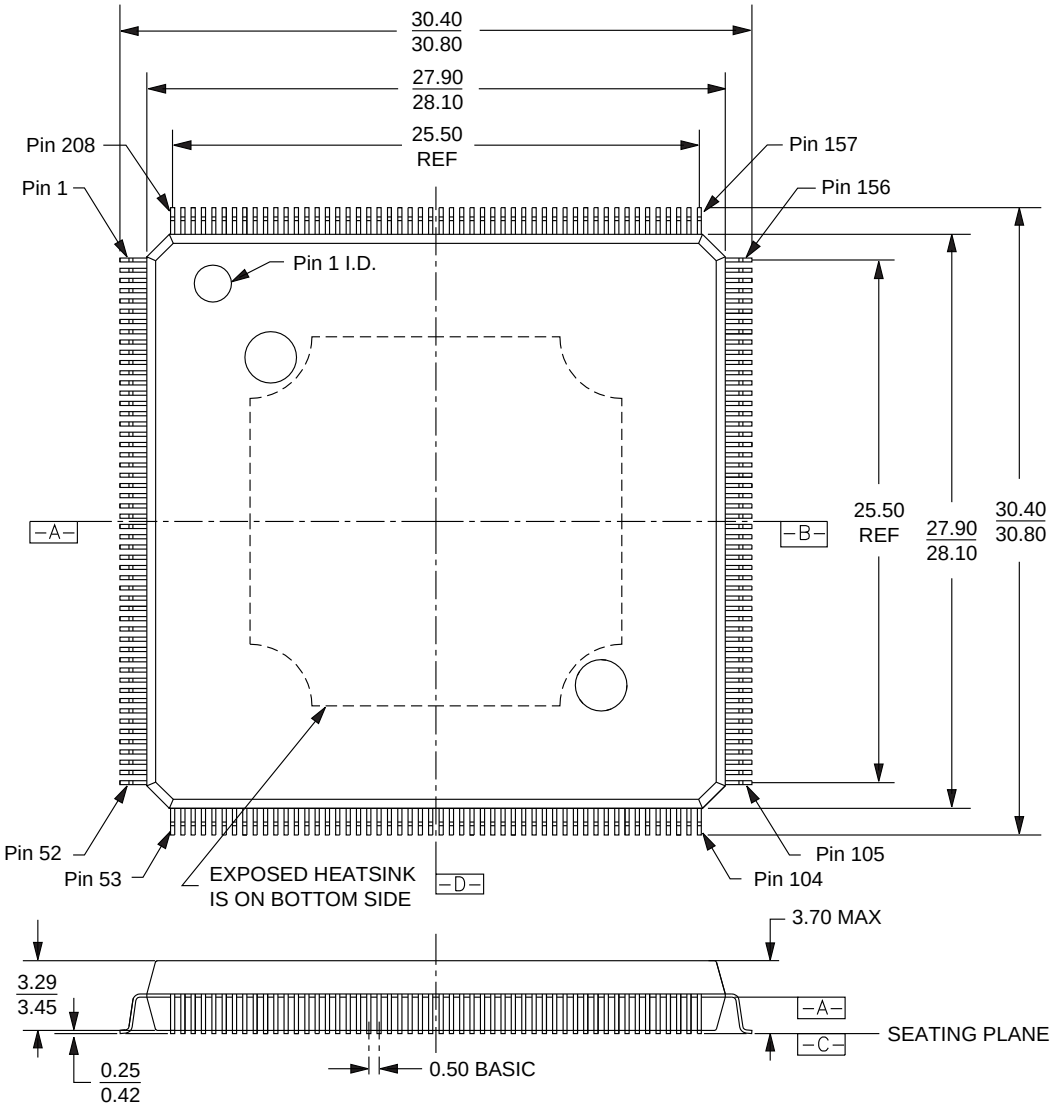



16-038-PQE160-1_AF
DT112
12-13-96 lv

# PHYSICAL DIMENSIONS

## PQE208

## 208-Pin Thin Quad Flat Pack; Trimmed and Formed (measured in millimeters)

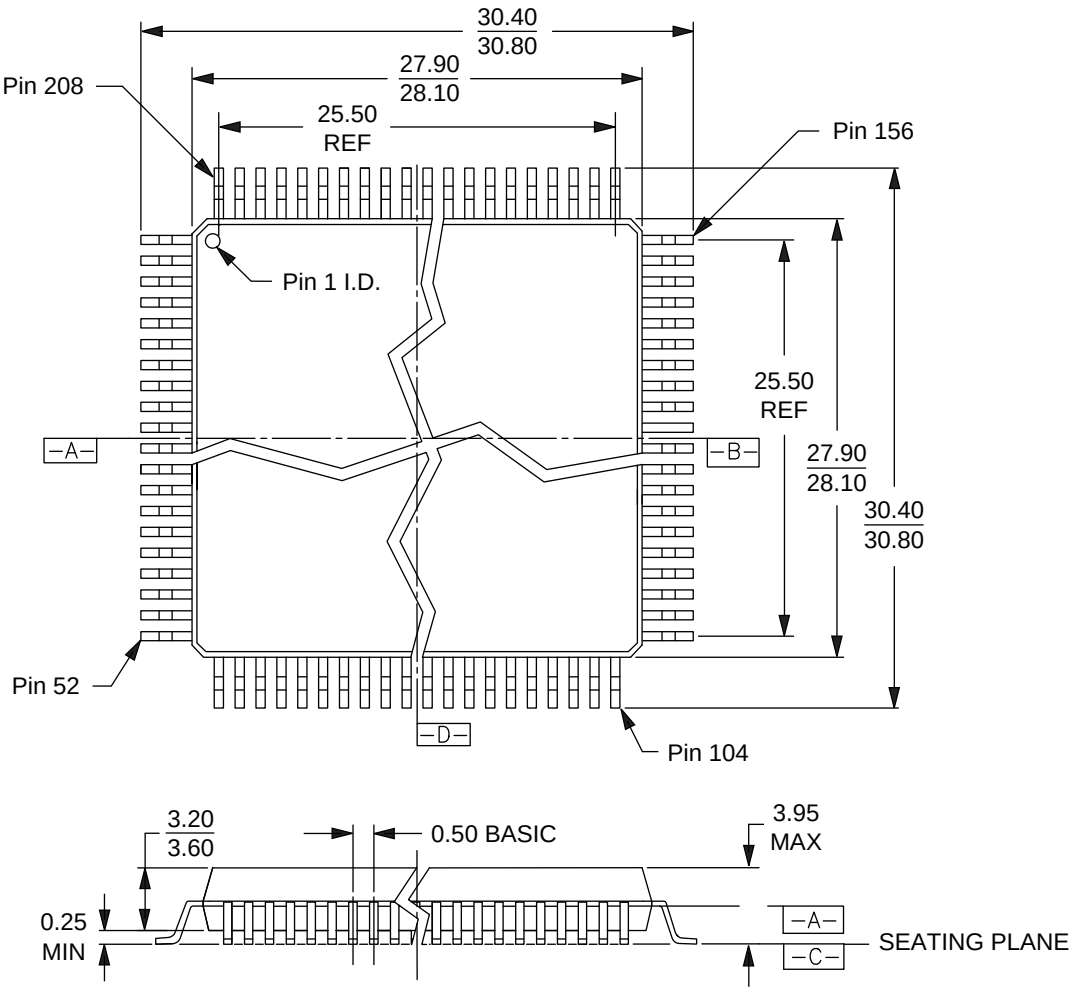



16-038-PQE208-1_AG
DT114
9-20-96 lv

# PHYSICAL DIMENSIONS

## PRH208

## 208-Pin Thin Quad Flat Pack; Trimmed and Formed (measured in millimeters)

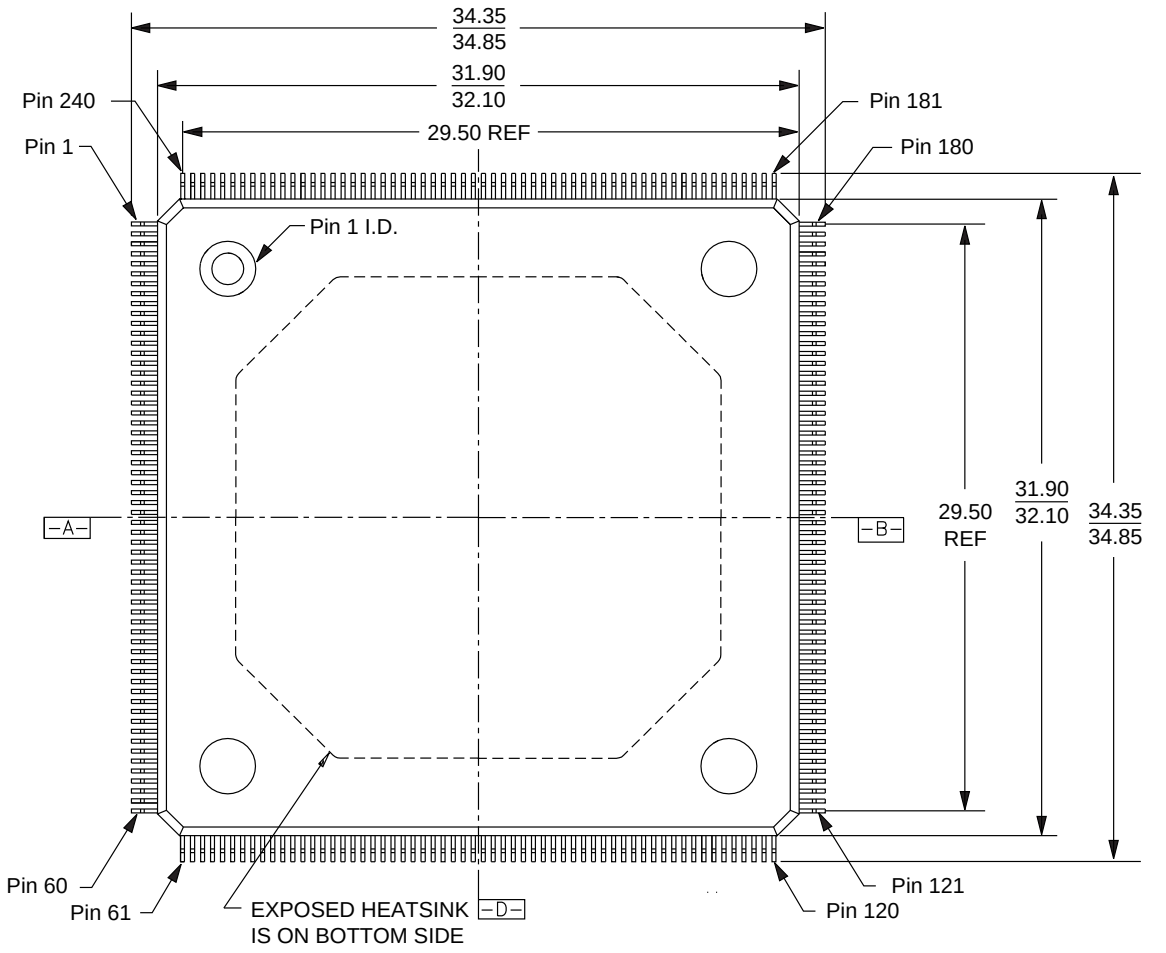


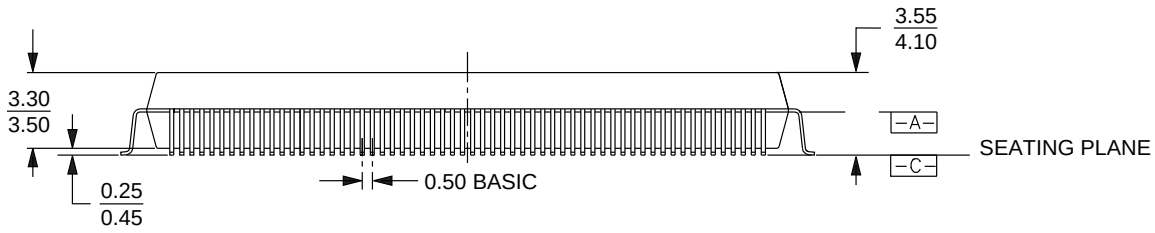

16-038-PQR-1_AH
PRH208
EC95
8-6-97 lv

# PHYSICAL DIMENSIONS

## PQE240

## 240-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)



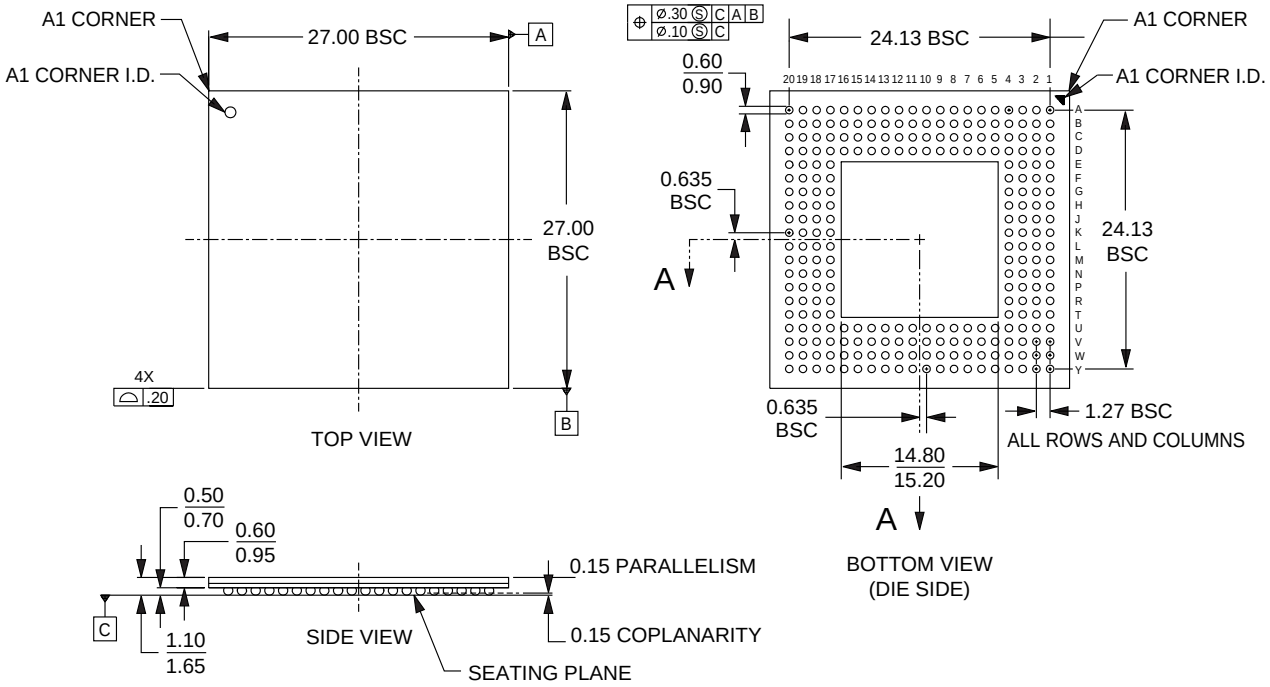




16-038-PQE240-3_AE
DT116
9-18-96 lv

# PHYSICAL DIMENSIONS

## BGD256

## 256-Pin Ball Grid Array (measured in millimeters)

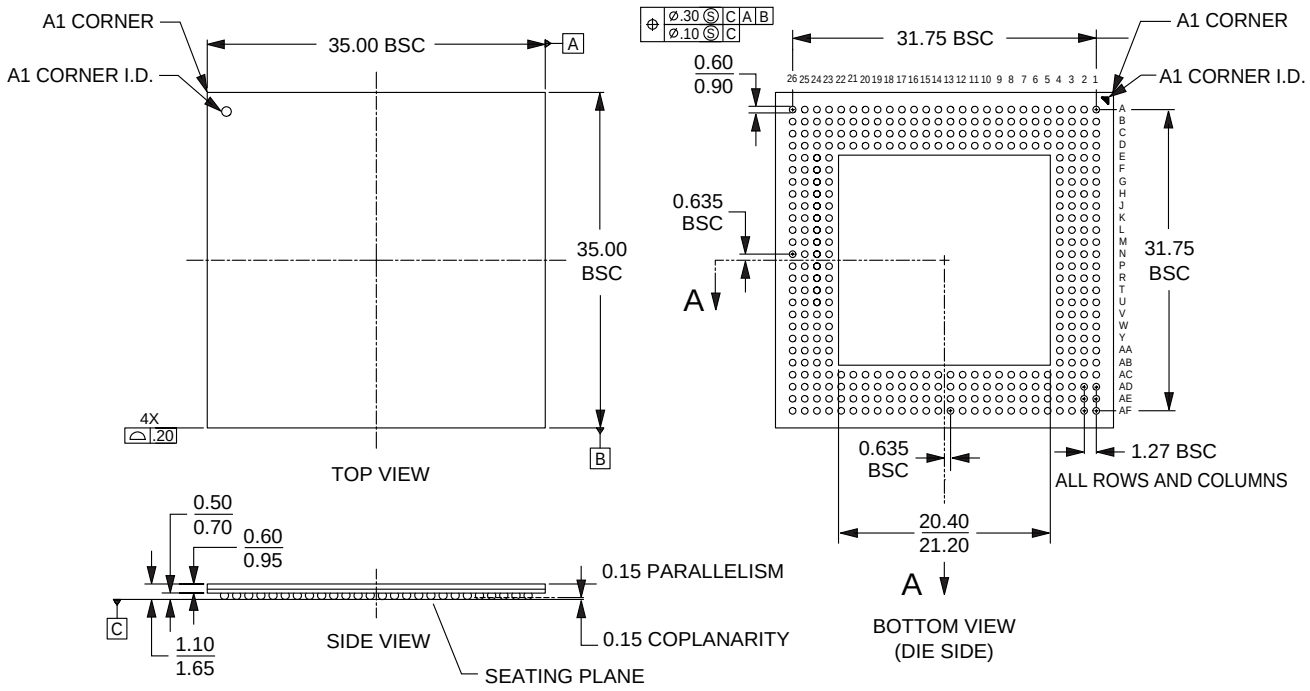



16-038-BGD256-1_AD
DT104
9-19-96 lv

# PHYSICAL DIMENSIONS

## BGD352

## 352-Pin Ball Grid Array (measured in millimeters)




16-038-BGD352-1_AE
DT106
9-19-96 lv