

Product Preview

8-Bit Serial or Parallel-Input/ Serial-Output Shift Register

High-Performance Silicon-Gate CMOS

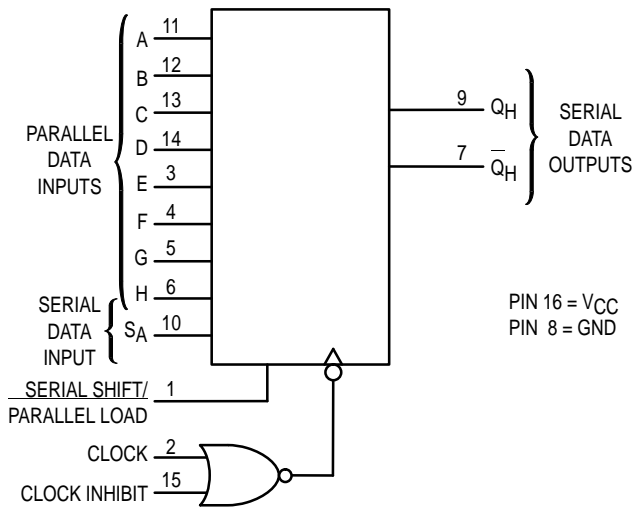
The MC54/74HC165A is identical in pinout to the LS165. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is an 8-bit shift register with complementary outputs from the last stage. Data may be loaded into the register either in parallel or in serial form. When the Serial Shift/Parallel Load input is low, the data is loaded asynchronously in parallel. When the Serial Shift/Parallel Load input is high, the data is loaded serially on the rising edge of either Clock or Clock Inhibit (see the Function Table).

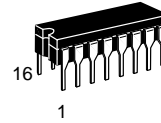
The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates

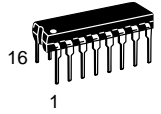
LOGIC DIAGRAM



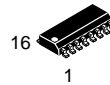
MC54/74HC165A



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-08



D SUFFIX
SOIC PACKAGE
CASE 751B-05

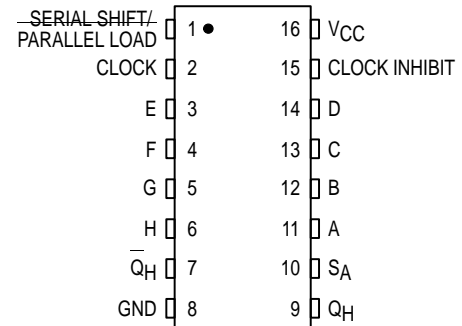


DT SUFFIX
TSSOP PACKAGE
CASE 948F-01

ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXAD	SOIC
MC74HCXXXADT	TSSOP

PIN ASSIGNMENT



FUNCTION TABLE

Inputs					Internal Stages		Output	Operation
Serial Shift/ Parallel Load	Clock	Clock Inhibit	SA	A - H	QA	QB	QH	
L	X	X	X	a ... h	a	b	h	Asynchronous Parallel Load
H	\nearrow	L	L	X	L	QAn	QGn	Serial Shift via Clock
H	\nearrow	L	H	X	H	QAn	QGn	
H	L	\nearrow	L	X	L	QAn	QGn	Serial Shift via Clock Inhibit
H	L	\nearrow	H	X	H	QAn	QGn	
H	X	H	X	X	No Change			Inhibited Clock
H	H	X	X	X	No Change			
H	L	L	X	X	No Change			No Clock

X = don't care QAn - QGn = Data shifted from the preceding stage

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.



MC54/74HC165A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
Ceramic DIP: - 10 mW/°C from 100° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 3.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	3.0	2.48	2.34	
4.5	3.98	3.84		3.70			
6.0	5.48	5.34		5.20			

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 8)	2.0	10	9	8	MHz
		3.0	15	14	12	
		4.5	30	28	25	
		6.0	50	45	40	
		6.0	50	45	40	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock (or Clock Inhibit) to Q _H or Q _H (Figures 1 and 8)	2.0	110	125	160	ns
		3.0	36	45	60	
		4.5	22	26	32	
		6.0	19	23	28	
		6.0	19	23	28	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q _H or Q _H (Figures 2 and 8)	2.0	85	96	106	ns
		3.0	57	63	71	
		4.5	25	29	32	
		6.0	19	23	27	
		6.0	19	23	27	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input H to Q _H or Q _H (Figures 3 and 8)	2.0	110	125	160	ns
		3.0	36	45	60	
		4.5	22	26	32	
		6.0	19	23	28	
		6.0	19	23	28	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	
		40	

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Parallel Data Inputs to Serial Shift/Parallel Load (Figure 4)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t_{su}	Minimum Setup Time, Input SA to Clock (or Clock Inhibit) (Figure 5)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t_{su}	Minimum Setup Time, Serial Shift/Parallel Load to Clock (or Clock Inhibit) (Figure 6)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t_{su}	Minimum Setup Time, Clock to Clock Inhibit (Figure 7)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t_h	Minimum Hold Time, Serial Shift/Parallel Load to Parallel Data Inputs (Figure 4)	2.0	1	1	1	ns
		3.0	1	1	1	
		4.5	1	1	1	
		6.0	1	1	1	
t_h	Minimum Hold Time, Clock (or Clock Inhibit) to Input SA (Figure 5)	2.0	1	1	1	ns
		3.0	1	1	1	
		4.5	1	1	1	
		6.0	1	1	1	
t_h	Minimum Hold Time, Clock (or Clock Inhibit) to Serial Shift/Parallel Load (Figure 6)	2.0	1	1	1	ns
		3.0	1	1	1	
		4.5	1	1	1	
		6.0	1	1	1	
t_{rec}	Minimum Recovery Time, Clock to Clock Inhibit (Figure 7)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t_w	Minimum Pulse Width, Clock (or Clock Inhibit) (Figure 1)	2.0	70	90	100	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
t_w	Minimum Pulse width, Serial Shift/Parallel Load (Figure 2)	2.0	70	90	100	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

A, B, C, D, E, F, G, H (Pins 11, 12, 13, 14, 3, 4, 5, 6)

Parallel Data inputs. Data on these inputs are asynchronously entered in parallel into the internal flip-flops when the Serial Shift/Parallel Load input is low.

SA (Pin 10)

Serial Data input. When the Serial Shift/Parallel Load input is high, data on this pin is serially entered into the first stage of the shift register with the rising edge of the Clock.

CONTROL INPUTS

Serial Shift/Parallel Load (Pin 1)

Data-entry control input. When a high level is applied to this pin, data at the Serial Data input (SA) are shifted into the register with the rising edge of the Clock. When a low level is

applied to this pin, data at the Parallel Data inputs are asynchronously loaded into each of the eight internal stages.

Clock, Clock Inhibit (Pins 2, 15)

Clock inputs. These two clock inputs function identically. Either may be used as an active-high clock inhibit. However, to avoid double clocking, the inhibit input should go high only while the clock input is high.

The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

OUTPUTS

QH, Q \bar{H} (Pins 9, 7)

Complementary Shift Register outputs. These pins are the noninverted and inverted outputs of the eighth stage of the shift register.

SWITCHING WAVEFORMS

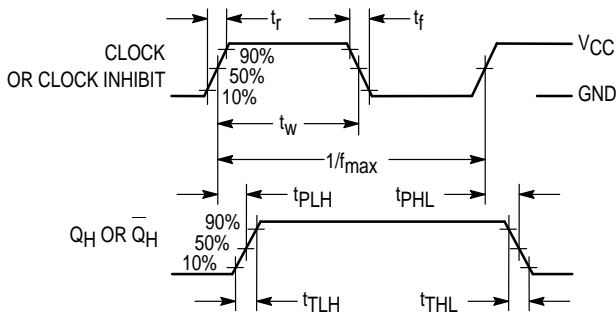


Figure 1. Serial-Shift Mode

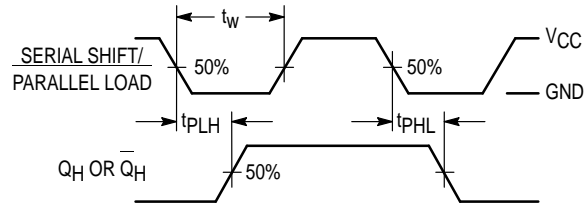


Figure 2. Parallel-Load Mode

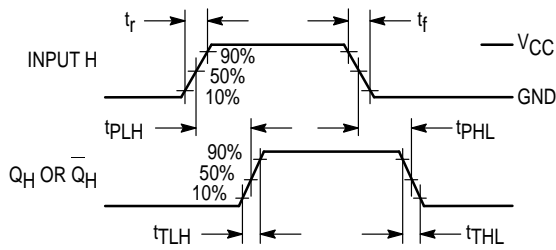


Figure 3. Parallel-Load Mode

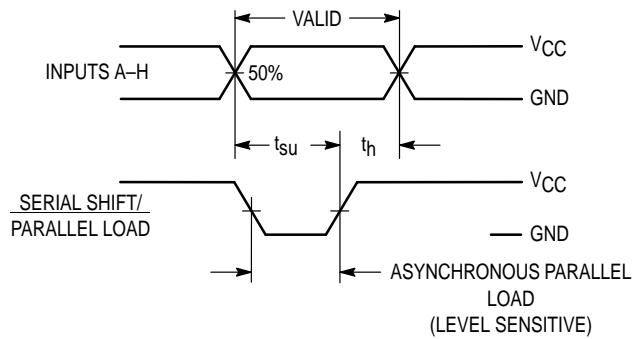


Figure 4. Parallel-Load Mode

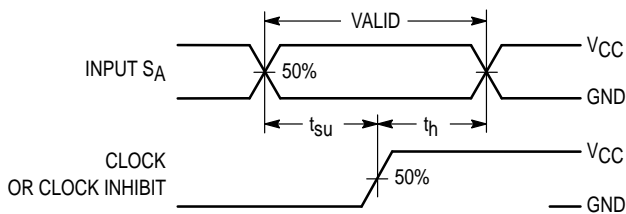


Figure 5. Serial-Shift Mode

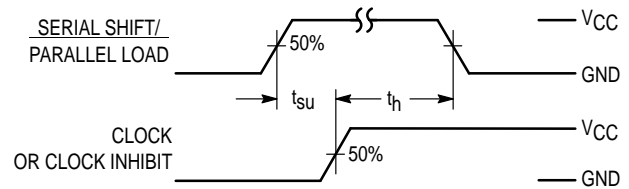


Figure 6. Serial-Shift Mode

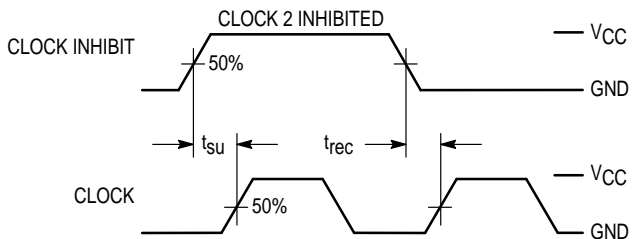
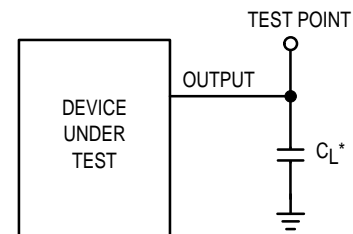


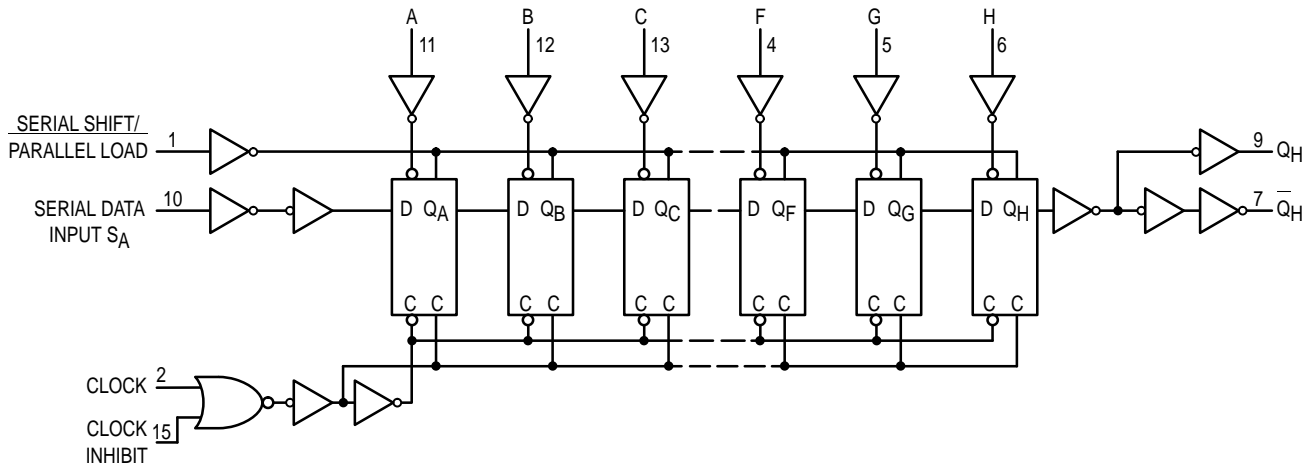
Figure 7. Serial-Shift, Clock-Inhibit Mode



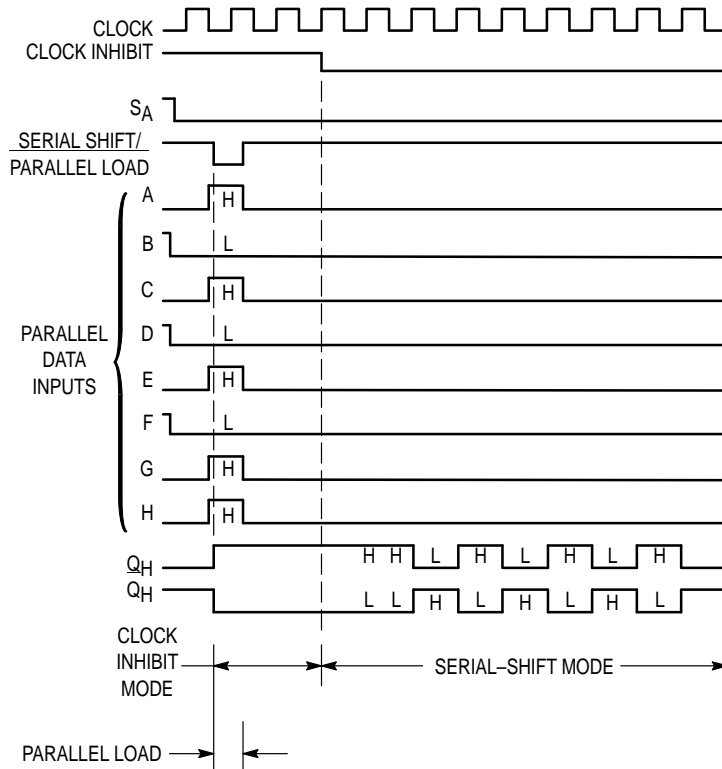
* Includes all probe and jig capacitance

Figure 8. Test Circuit

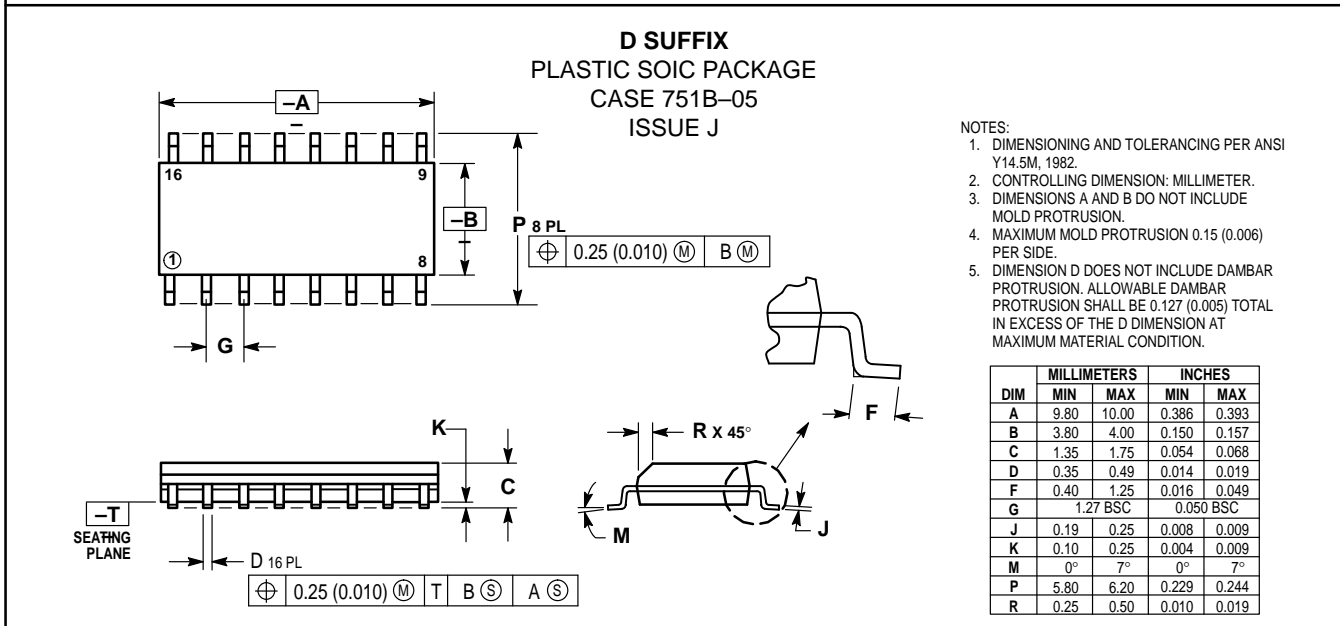
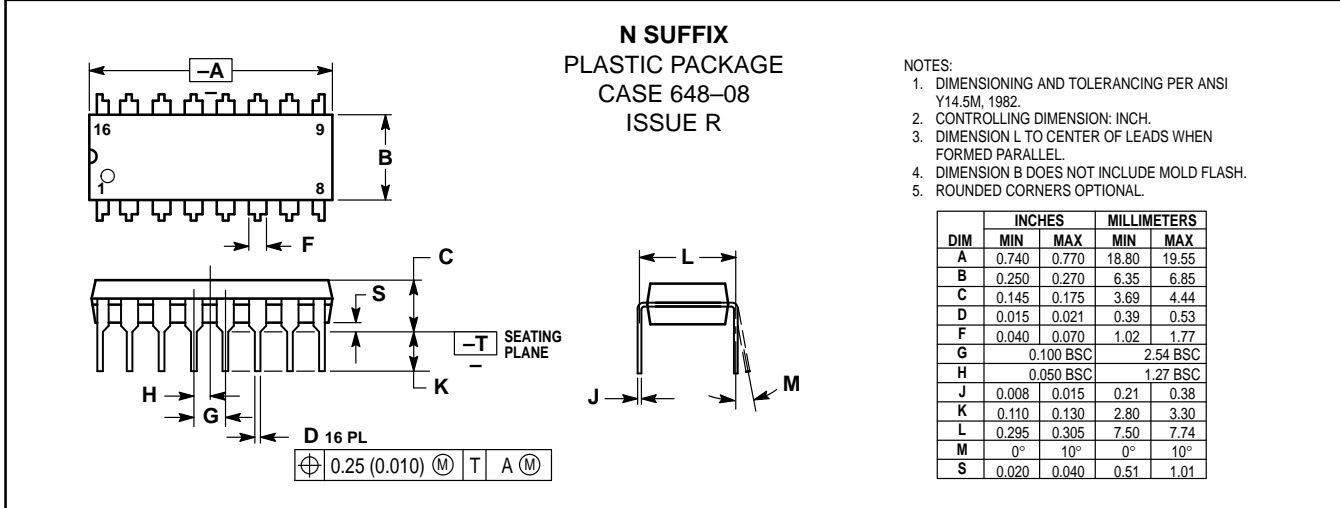
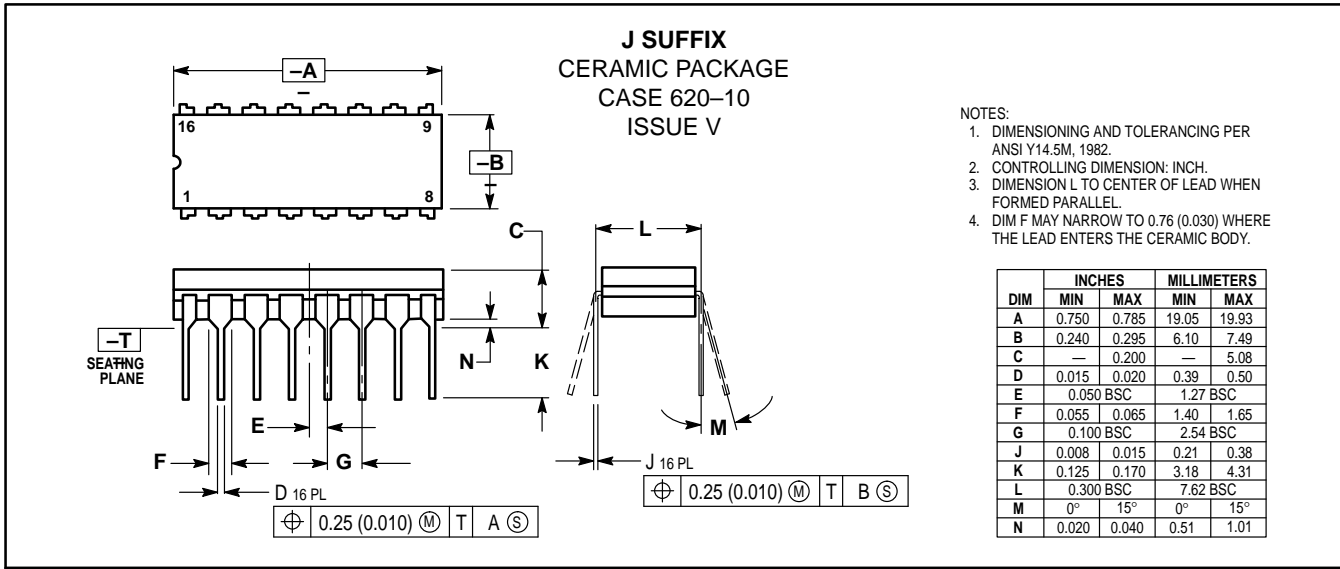
EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM

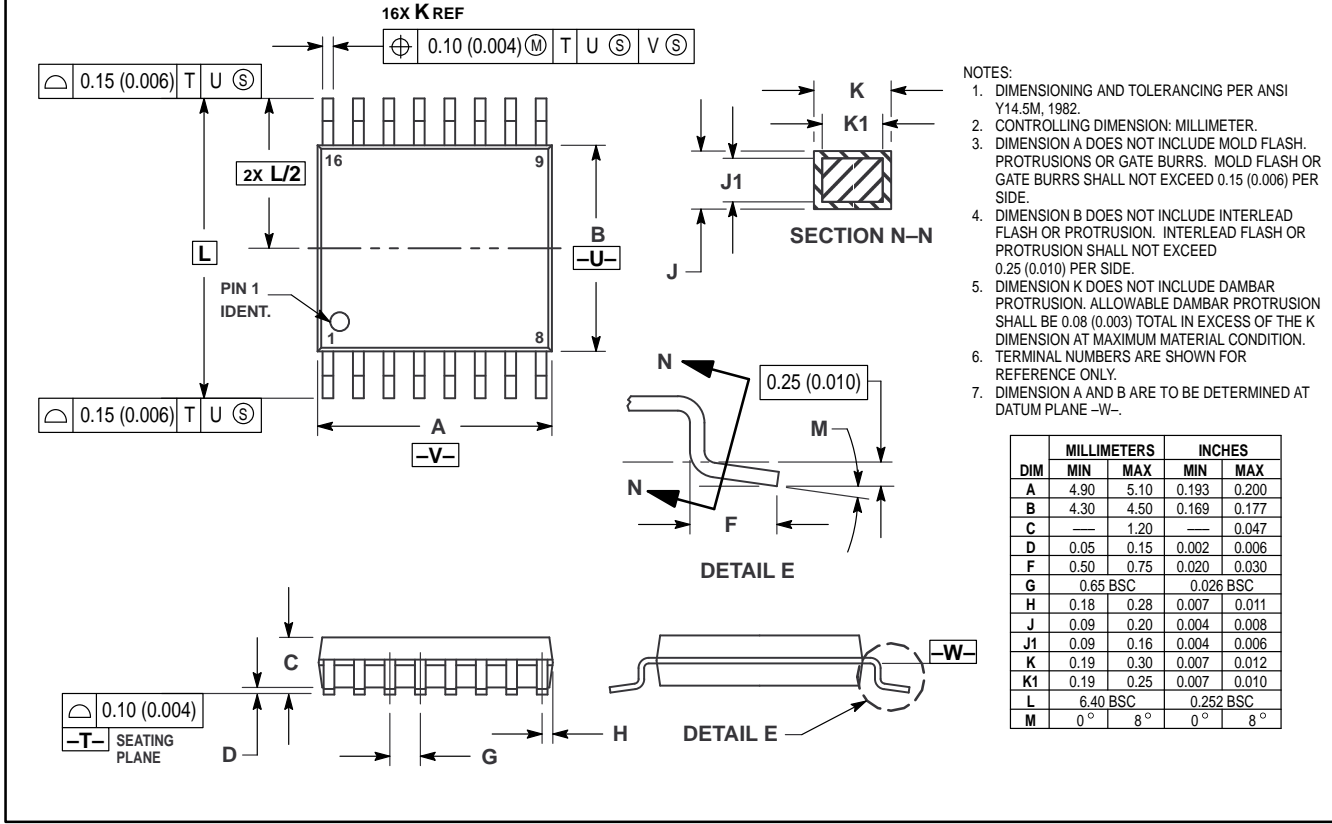


OUTLINE DIMENSIONS



OUTLINE DIMENSIONS

DT SUFFIX
 PLASTIC TSSOP PACKAGE
 CASE 948F-01
 ISSUE O



Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:
 USA/EUROPE: Motorola Literature Distribution;
 P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,
 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

MFAX: RMFAX0@email.sps.mot.com -TOUCHTONE (602) 244-6609
 INTERNET: http://Design-NET.com

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



CODELINE

MC54/74HC165A/D

