

Decade Counter

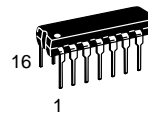
High-Performance Silicon-Gate CMOS

The MC74HC4017 is identical in pinout to the standard CMOS MC14017B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

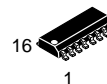
The HC4017 uses a five stage Johnson counter and decoding logic to provide high-speed operation. This device also has an active-high, as well as active-low clock input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 176 FETs or 44 Equivalent Gates

MC74HC4017



N SUFFIX
PLASTIC PACKAGE
CASE 648-08

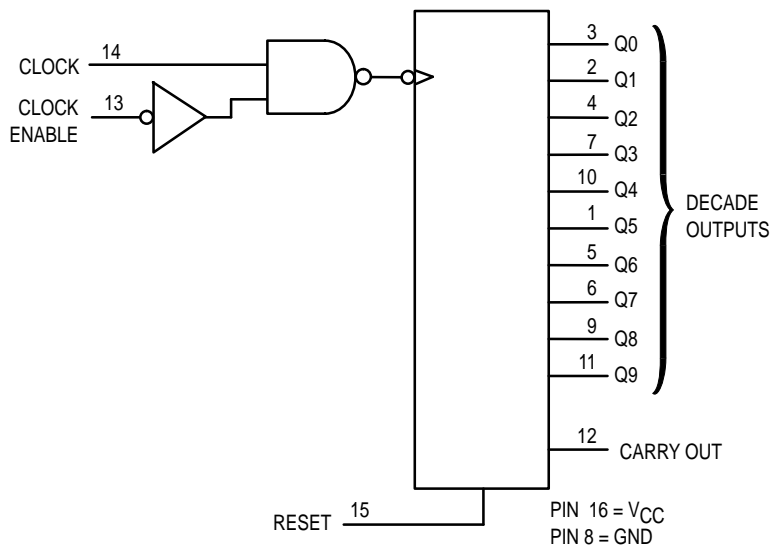


D SUFFIX
SOIC PACKAGE
CASE 751B-05

ORDERING INFORMATION

MC74HCXXXXN Plastic
MC74HCXXXXD SOIC

LOGIC DIAGRAM



PIN ASSIGNMENT

Q5	1	16	VCC
Q1	2	15	RESET
Q0	3	14	CLOCK
Q2	4	13	CLOCK ENABLE
Q6	5	12	CARRY OUT
Q7	6	11	Q9
Q3	7	10	Q4
GND	8	9	Q8



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25° C	≤ 85° C	≤ 125° C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 9)	2.0	4.0	3.2	2.6	MHz
		4.5	20	16	13	
		6.0	24	19	15	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 9)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Carry Out (Figures 2 and 9)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Reset to Q (Figures 3 and 9)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t _{PLH}	Maximum Propagation Delay, Reset to Carry Out (Figures 3 and 9)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock Enable to Q (Figures 4 and 9)	2.0	250	315	375	ns
		4.5	50	63	75	
		6.0	43	54	64	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock Enable to Carry Out (Figures 5 and 9)	2.0	250	315	375	ns
		4.5	50	63	75	
		6.0	43	54	64	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 8 and 9)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	





* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Clock Enable to Clock (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t_{su}	Minimum Setup Time, Clock Enable to Clock (Inhibit Count) (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t_h	Minimum Hold Time, Clock to Clock Enable (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t_{rec}	Minimum Recovery Time, Reset to Clock (Figure 7)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t_w	Minimum Pulse Width, Clock Input (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_w	Minimum Pulse Width, Reset Input (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_w	Minimum Pulse Width, Clock Enable Input (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

FUNCTION TABLE

Clock	Clock Enable	Reset	Output State*
L	X	L	no change
X	H	L	no change
X	X	H	reset counter, Q0 = H, Q1–Q9 = L, C0 = H
	L	L	advance to next state
	X	L	no change
X		L	no change
H		L	advance to next state

X = Don't care

* Carry Out = H for Q0, Q1, Q2, Q3, or Q4 = H; Carry Out = L otherwise.

PIN DESCRIPTIONS

INPUTS

Clock (Pin 14)

Counter clock input. While Clock Enable is low, a low-to-high transition on this input advances the counter to its next state.

Reset (Pin 15)

Asynchronous counter reset input. A high level at this input initializes the counter and forces Q0 and Carry Out to a high, Q1–Q9 are forced to a low level.

Clock Enable (Pin 13)

Active-low clock enable input. A low level on this input allows the device to count. A high level on this input inhibits the counting operation. This input may also be used as a

negative-edge clock input. using Clock (Pin 14) as an active-high enable pin.

OUTPUTS

Q0–Q9 (Pins 3, 2, 4, 7, 10, 1, 5, 6, 9, 11)

Decoded decade counter outputs. Each of these outputs is high for one clock period only.

Carry Out (Pin 12)

Cascading output pin. This output is used either as a cascading output or a symmetrical divide-by-ten output. This output goes low when a count of five is reached and high when the counter advances to zero or when reset. When the counters are cascaded this output provides a rising-edge signal for the clock input of the next counter stage.

SWITCHING WAVEFORMS

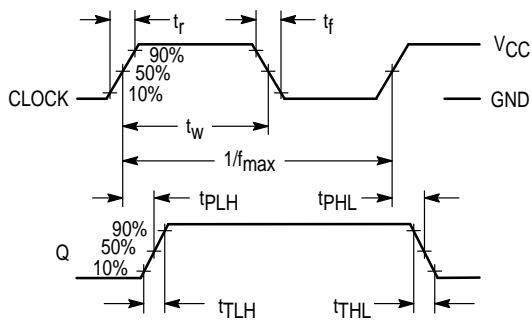


Figure 1.

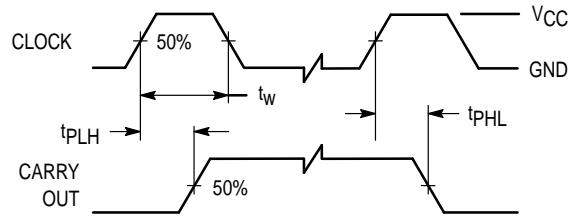


Figure 2.

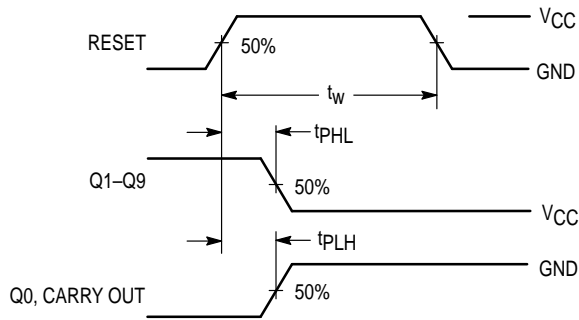


Figure 3.

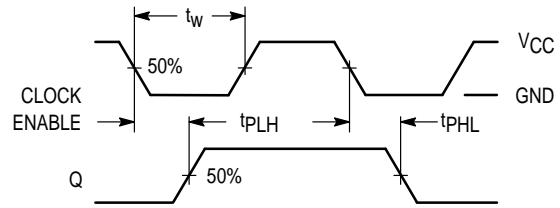


Figure 4.

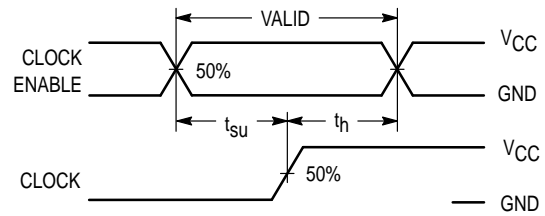


Figure 6.

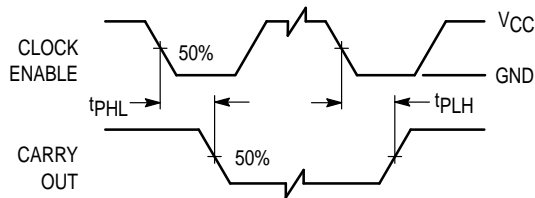


Figure 5.

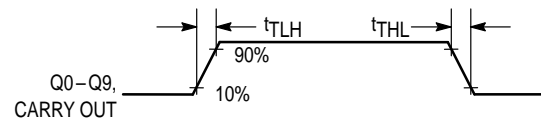


Figure 8.

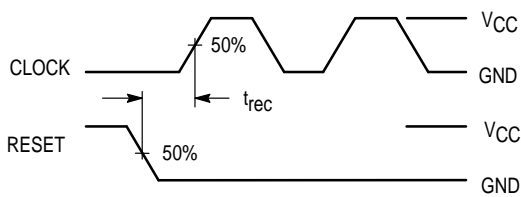
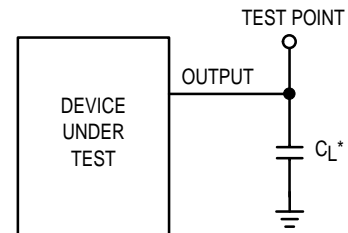


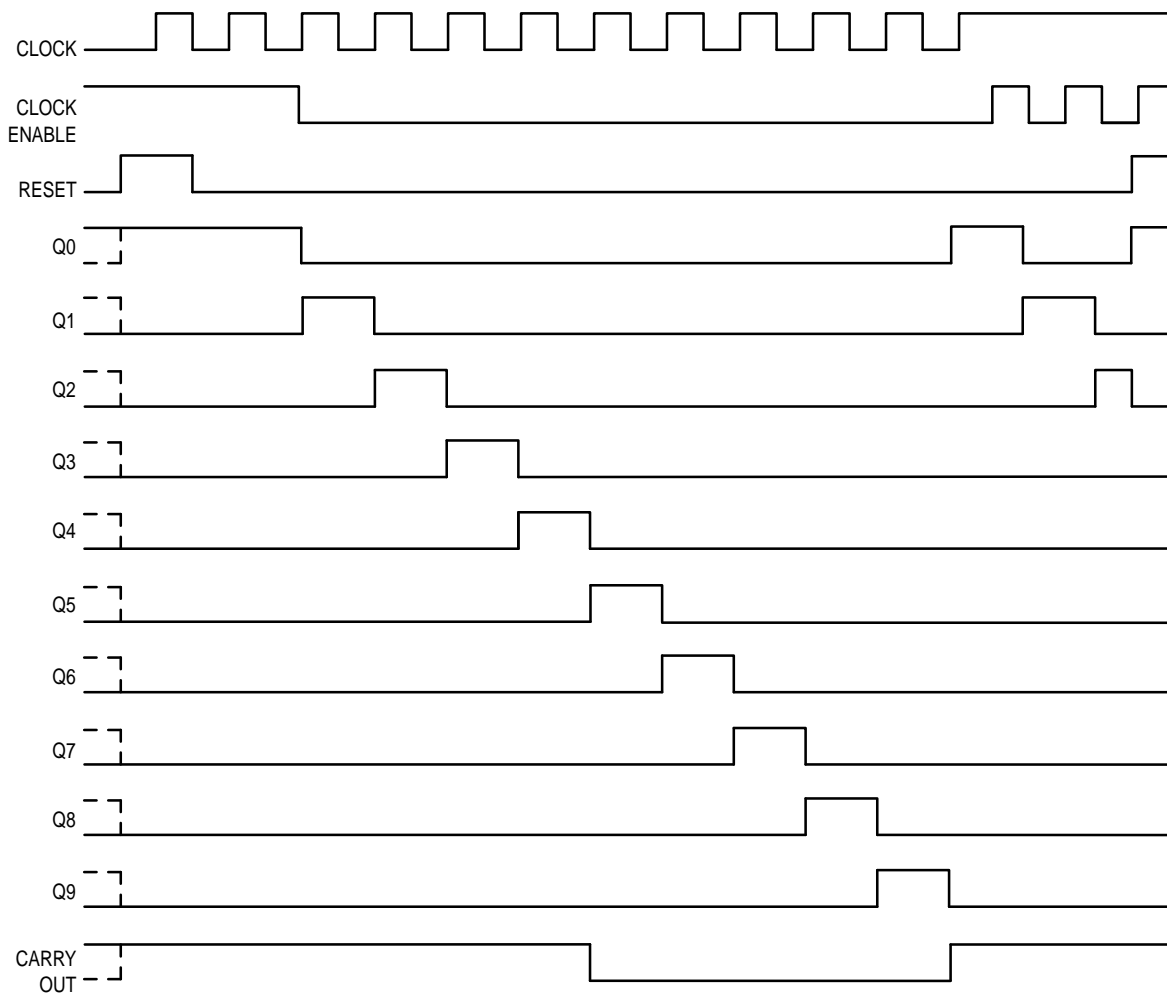
Figure 7.



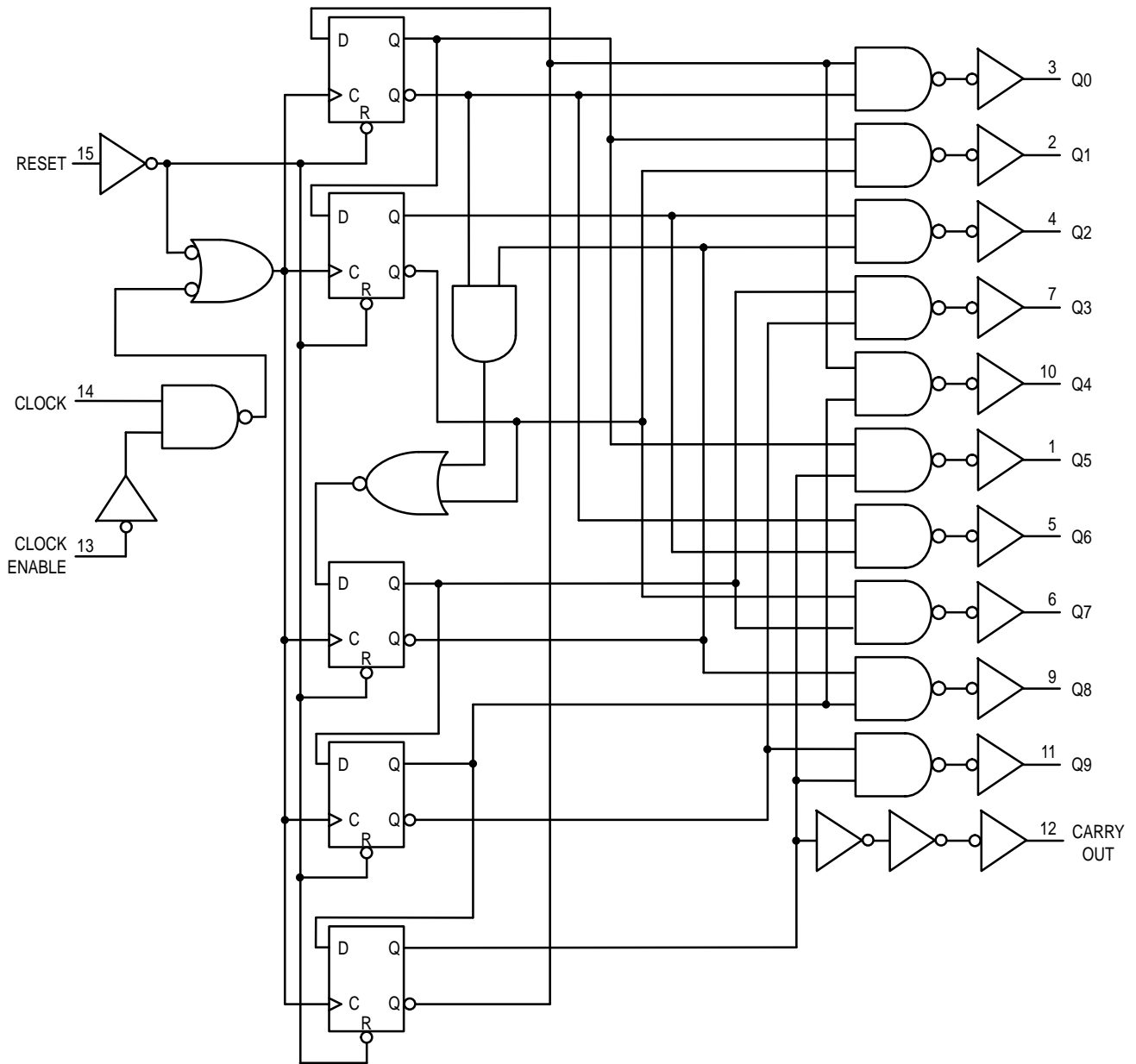
* Includes all probe and jig capacitance

Figure 9. Test Circuit

TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM



TYPICAL APPLICATIONS

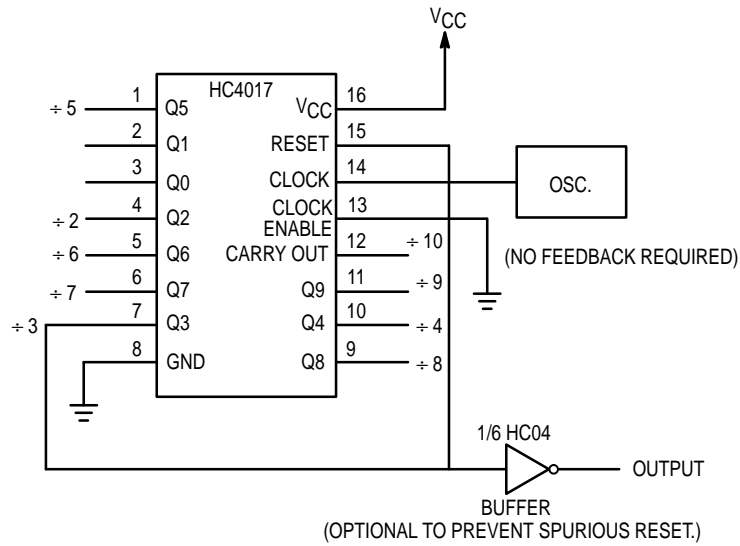


Figure 10 shows a divide by 2 through 10 circuit using one HC4017. Please note that since Reset is asynchronous, the output pulse widths are narrow.

Figure 10. ÷2 Through ÷ 10 Circuit

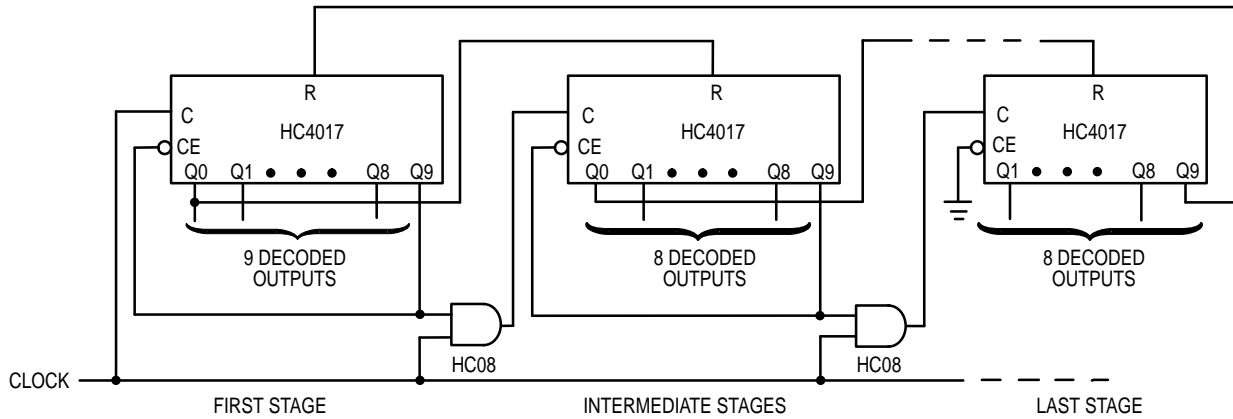
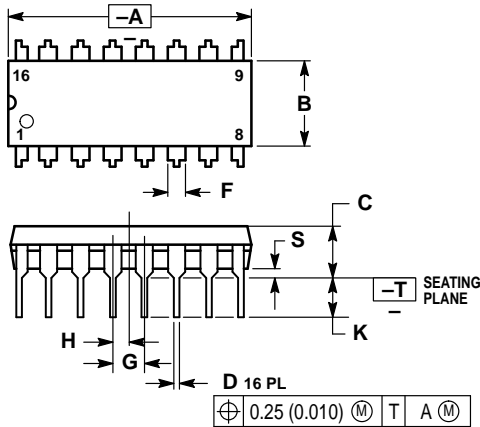


Figure 11 shows a technique for cascading the counters to extend the number of decoded output states. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

Figure 11. Counter Expansion

OUTLINE DIMENSIONS

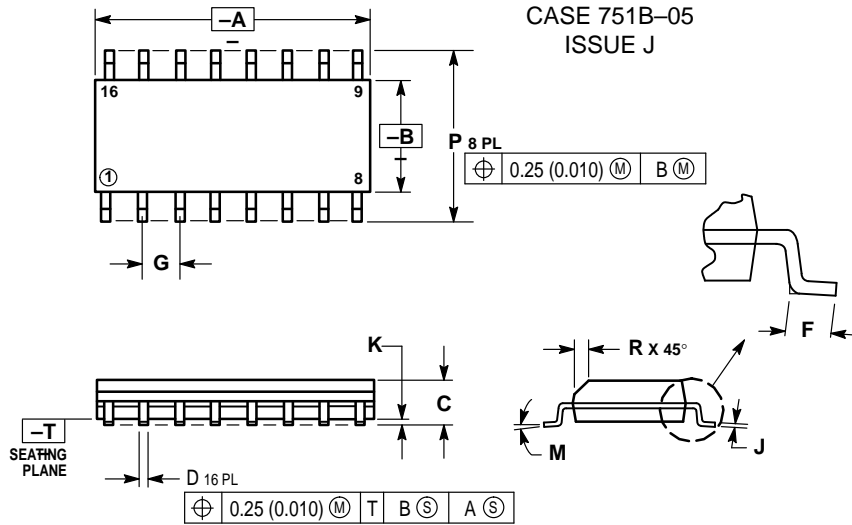
N SUFFIX
PLASTIC PACKAGE
CASE 648-08
ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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