High–Performance Silicon–Gate CMOS

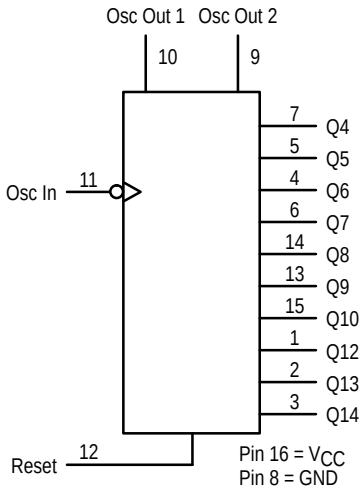
The MC54/74C4060A is identical in pinout to the standard CMOS MC14060B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 14 master–slave flip–flops and an oscillator with a frequency that is controlled either by a crystal or by an RC circuit connected externally. The output of each flip–flop feeds the next and the frequency at each output is half of that of the preceding one. The state of the counter advances on the negative–going edge of the Osc In. The active–high Reset is asynchronous and disables the oscillator to allow very low power consumption during stand–by operation.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with Osc Out 2 of the HC4060A.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With JEDEC Standard No. 7A Requirements
- Chip Complexity: 390 FETs or 97.5 Equivalent Gates

LOGIC DIAGRAM



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AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns) **– continued**

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

* For T_A = 25°C and C_L = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

V_{CC} = 2.0 V: t_P = [93.7 + 59.3 (n–1)] ns
V_{CC} = 3.0 V: t_P = [61.5+ 34.4 (n–1)] ns
V_{CC} = 4.5 V: t_P = [30.25 + 14.6 (n–1)] ns
V_{CC} = 6.0 V: t_P = [24.4 + 12 (n–1)] ns

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	35	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		3.0	75	100	120	
		4.5	20	25	30	
		6.0	17	21	25	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	23	
		6.0	13	16	19	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	23	
		6.0	13	16	19	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

Osc In (Pin 11)

Negative–edge triggering clock input. A high–to–low transition on this input advances the state of the counter. Osc In may be driven by an external clock source.

Reset (Pin 12)

Active–high reset. A high level applied to this input asynchronously resets the counter to its zero state (forcing all Q outputs low) and disables the oscillator.

OUTPUTS

Q4—Q10, Q12–Q14 (Pins 7, 5, 4, 6, 13, 15, 1, 2, 3)

Active–high outputs. Each Qn output divides the Clock input frequency by 2^N. The user should note the Q1, Q2, Q3 and Q11 are not available as outputs.

Osc Out 1, Osc Out 2 (Pins 9, 10)

Oscillator outputs. These pins are used in conjunction with Osc In and the external components to form an oscillator (See NO TAG and NO TAG). When Osc In is being driven with an external clock source, Osc Out 1 and Osc Out 2 must be left open circuited. With the crystal oscillator configuration in Figure 6, Osc Out 2 must be left open circuited.

SWITCHING WAVEFORMS

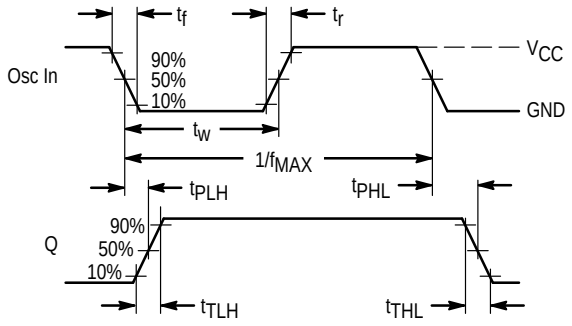


Figure 1.

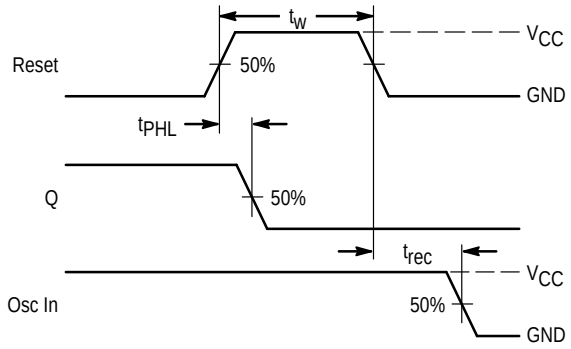


Figure 2.

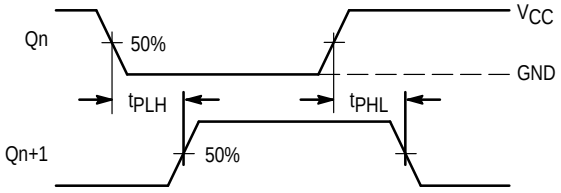
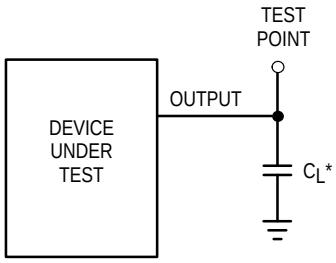


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

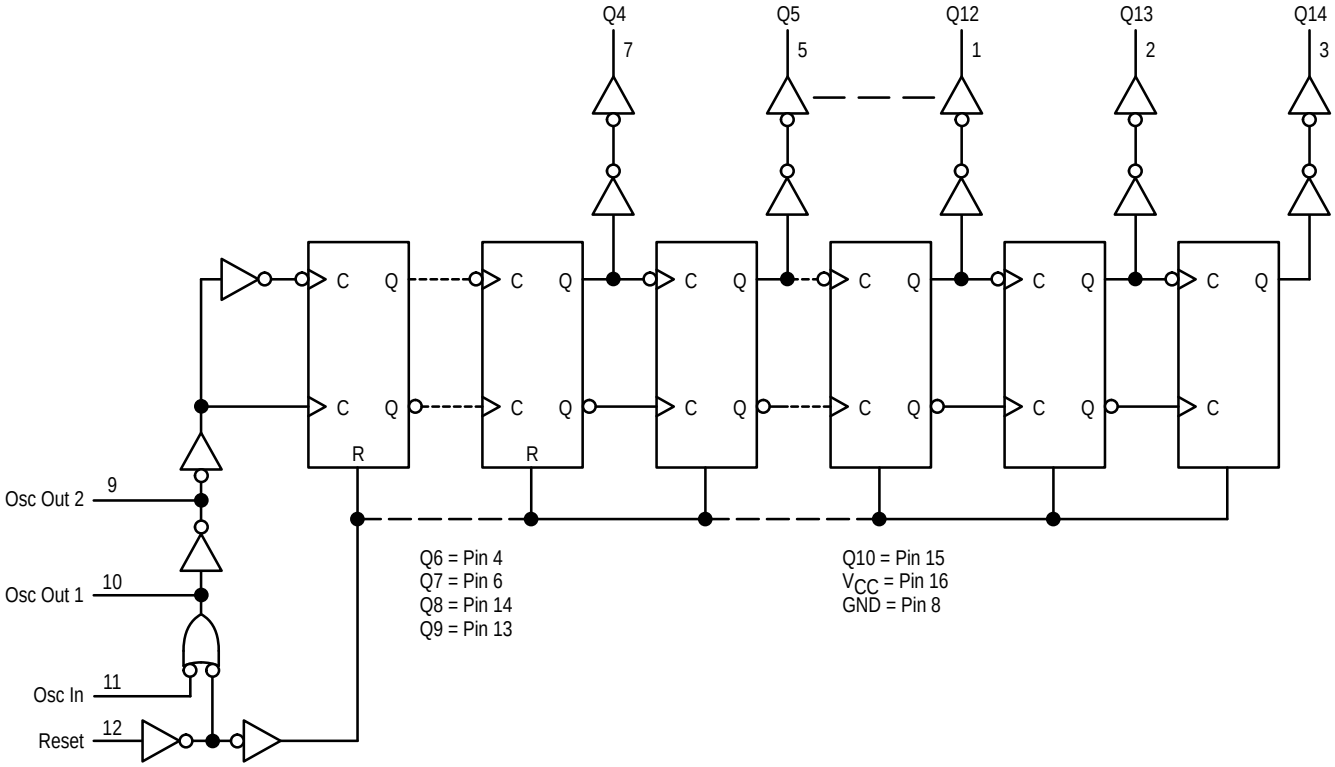
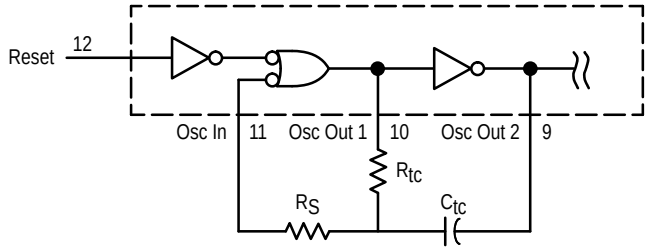


Figure 5. Expanded Logic Diagram



For $2.0V \le V_{CC} \le 6.0V$
$10R_{tc} > R_S > 2R_{tc}$
$400Hz \le f \le 400Khz$:

$$f \approx \frac{1}{3\ R_{tc}C_{tc}}$$ (f in Hz, R_{tc} in ohms, C_{tc} in farads)

The formula may vary for other frequencies.

Figure 6. Oscillator Circuit Using RC Configuration

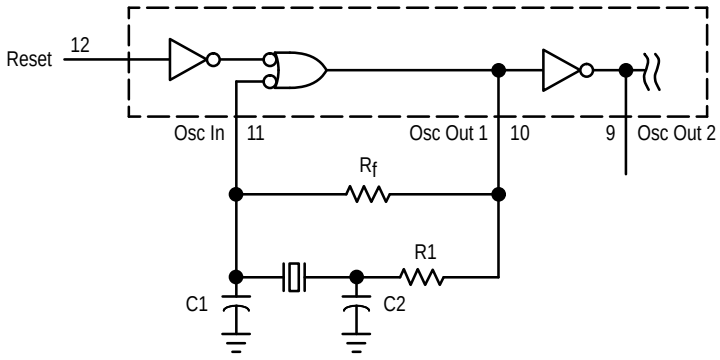
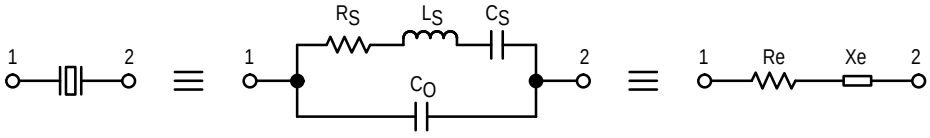


Figure 7. Pierce Crystal Oscillator Circuit

TABLE 1. CRYSTAL OSCILLATOR AMPLIFIER SPECIFICATIONS (T_A = 25°C; Input = Pin 11, Output = Pin 10)

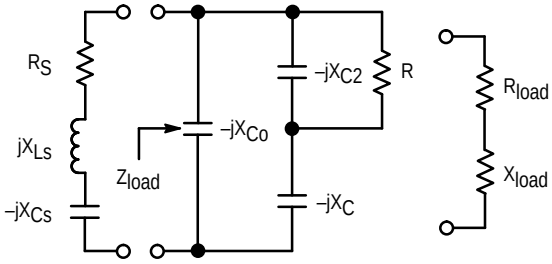
Type		Positive Reactance (Pierce)
Input Resistance, R_{in}		60MΩ Minimum
Output Impedance, Z_{out} (4.5V Supply)		200Ω (See Text)
Input Capacitance, C_{in}		5pF Typical
Output Capacitance, C_{out}		7pF Typical
Series Capacitance, C_a		5pF Typical
Open Loop Voltage Gain with Output at Full Swing, α	3Vdc Supply 4Vdc Supply 5Vdc Supply 6Vdc Supply	5.0 Expected Minimum 4.0 Expected Minimum 3.3 Expected Minimum 3.1 Expected Minimum

PIERCE CRYSTAL OSCILLATOR DESIGN



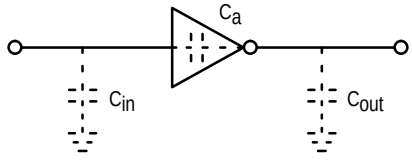
Value are supplied by crystal manufacturer (parallel resonant crystal).

Figure 8. Equivalent Crystal Networks



NOTE: C = C1 + C_{in} and R = R1 + R_{out}. C_o is considered as part of the load. C_a and R_f typically have minimal effect below 2MHz.

Figure 9. Series Equivalent Crystal Load



Values are listed in Table 1.

Figure 10. Parasitic Capacitances of the Amplifier

DESIGN PROCEDURES

The following procedure applies for oscillators operating below 2MHz where Z is a resistor R1. Above 2MHz, additional impedance elements should be considered: C_{out} and C_a of the amp, feedback resistor R_f, and amplifier phase shift error from 180°C.

Step 1: Calculate the equivalent series circuit of the crystal at the frequency of oscillation.

$$Z_e = \frac{-jX_{C_0}(R_S + jX_{L_S} - jX_{C_S})}{-jX_{C_0} + R_S + jX_{L_S} - jX_{C_S}} = R_e + jX_e$$

Reactance jX_e should be positive, indicating that the crystal is operating as an inductive reactance at the oscillation frequency. The maximum R_S for the crystal should be used in the equation.

Step 2: Determine β, the attenuation, of the feedback network. For a closed-loop gain of 2, $A_V\beta = 2, \beta = 2/A_V$ where A_V is the gain of the HC4060A amplifier.

Step 3: Determine the manufacturer's loading capacitance. For example: A manufacturer may specify an external load capacitance of 32pF at the required frequency.

Step 4: Determine the required Q of the system, and calculate R_{load}, For example, a manufacturer specifies a crystal Q of 100,000. In-circuit Q is arbitrarily set at 20% below crystal Q or 80,000. Then $R_{load} = (2\pi f_o L_S/Q) - R_S$ where L_S and R_S are crystal parameters.

Step 5: Simultaneously solve, using a computer,

$$\beta = \frac{X_C \cdot X_{C2}}{R \cdot R_e + X_{C2}\,(X_e - X_C)} \quad \text{(with feedback phase shift = 180°)} \qquad (\text{Eq 1})$$

$$X_e = X_{C2} + X_C + \frac{R_e X_{C2}}{R} = X_{C_{load}} \quad \text{(where the loading capacitor is an external load, not including } C_o) \qquad (\text{Eq 2})$$

$$R_{load} = \frac{RX_{C_0}X_{C2}\,[(X_C + X_{C2})(X_C + X_{C_0}) - X_C(X_C + X_{C_0} + X_{C2})]}{X^2_{C2}(X_C + X_{C_0})^2 + R^2(X_C + X_{C_0} + X_{C2})^2} \qquad (\text{Eq 3})$$

Here $R = R_{out} + R1$. R_{out} is amp output resistance, R1 is Z. The C corresponding to X_C is given by $C = C1 + C_{in}$.

Alternately, pick a value for R1 (i.e, let $R1 = R_S$). Solve Equations 1 and 2 for C1 and C2. Use Equation 3 and the fact that $Q = 2\pi f_o L_S/(R_S + R_{load})$ to find in-circuit Q. If Q is not satisfactory pick another value for R1 and repeat the procedure.

CHOOSING R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 limits the drive level.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at Osc Out 2 (Pin 9). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

SELECTING R_f

The feedback resistor, R_f, typically ranges up to 20MΩ. R_f determines the gain and bandwidth of the amplifier. Proper bandwidth insures oscillation at the correct frequency plus roll-off to minimize gain at undesirable frequencies, such as the first overtone. R_f must be large enough so as to not affect the phase of the feedback network in an appreciable manner.

ACKNOWLEDGEMENTS AND RECOMMENDED REFERENCES

The following publications were used in preparing this data sheet and are hereby acknowledged and recommended for reading:

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

D. Babin, "Designing Crystal Oscillators", Machine Design, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", Machine Design, April 25, 1985.

ALSO RECOMMENDED FOR READING:

E. Hafner, "The Piezoelectric Crystal Unit-Definitions and Method of Measurement", Proc. IEEE, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", Electro-Technology, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", Electronic Design, May, 1966.

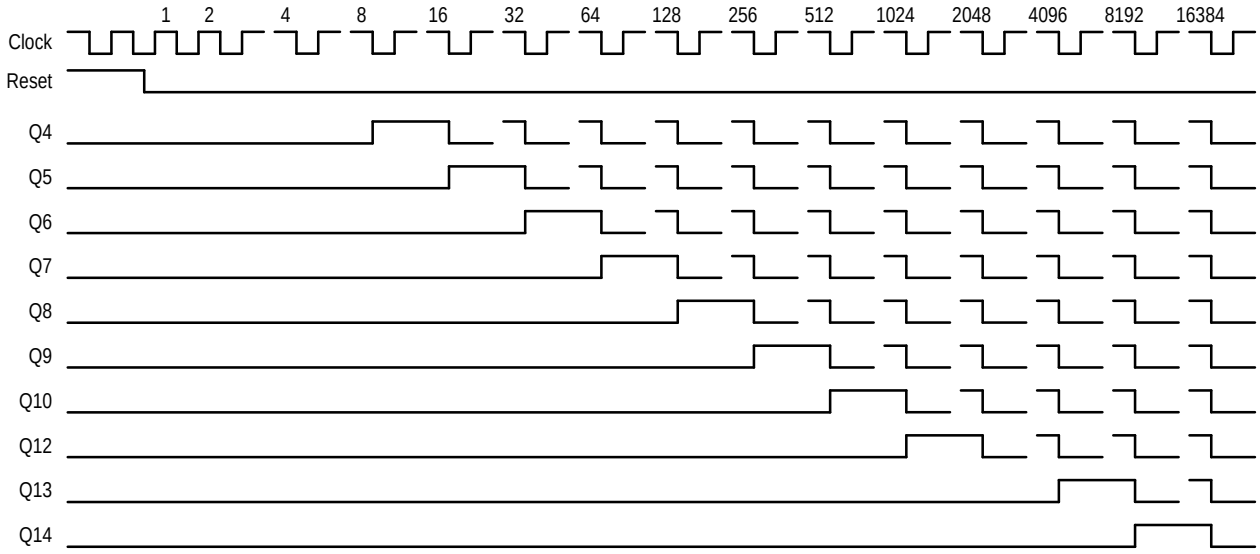
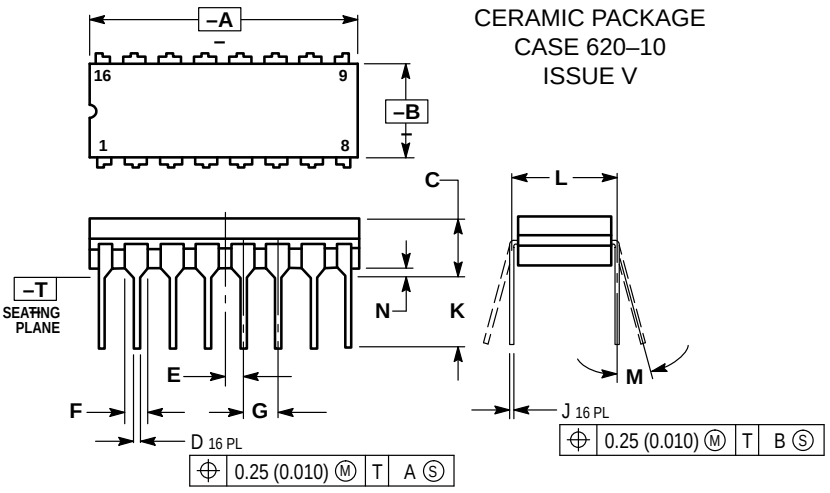


Figure 11. Timing Diagram

OUTLINE DIMENSIONS

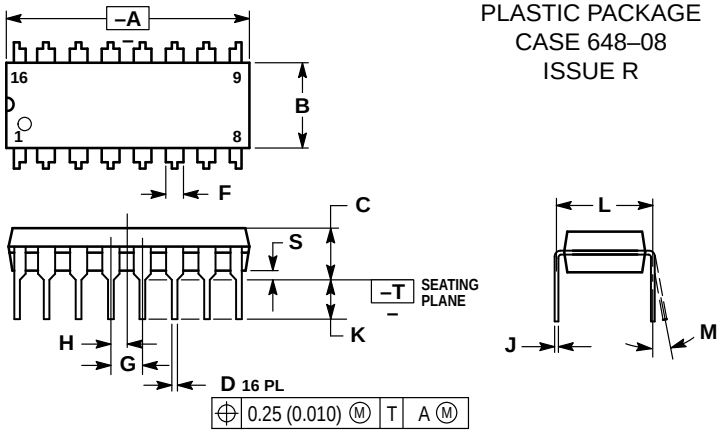
J SUFFIX
CERAMIC PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

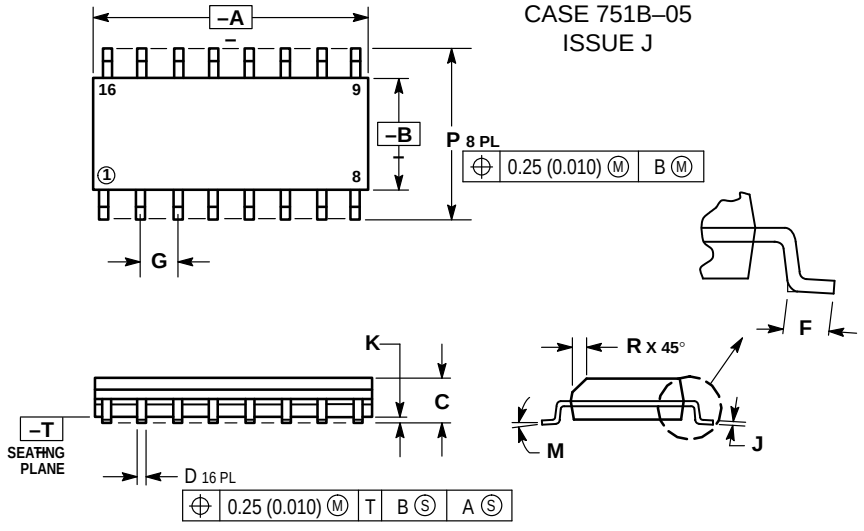
N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

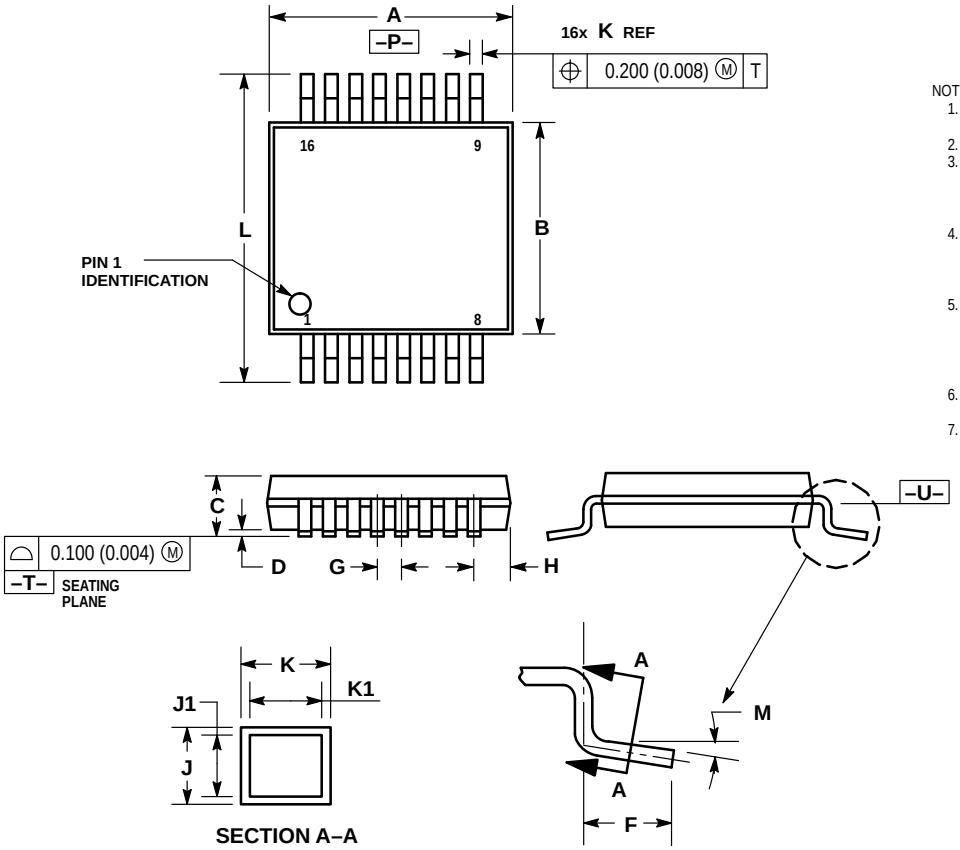


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

OUTLINE DIMENSIONS

DT SUFFIX
TSSOP PACKAGE
CASE 948C–03
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –U–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	——	5.10	——	0.200
B	4.30	4.50	0.169	0.177
C	——	1.20	——	0047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.22	0.23	0.009	0.010
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0°	10°	0°	10°

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