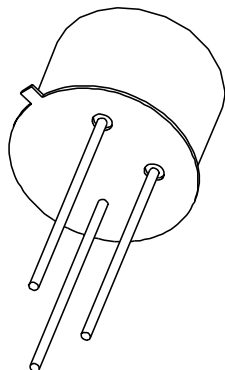


DATA SHEET



BSS61; BSS62 PNP Darlington transistors

Product specification
Supersedes data of September 1994
File under Discrete Semiconductors, SC04

1997 May 14

PNP Darlington transistors

BSS61; BSS62

FEATURES

- High current (max. 1 A)
- Low voltage (max. 80 V)
- Integrated diode and resistor.

APPLICATIONS

- Industrial high gain amplification.

DESCRIPTION

PNP Darlington transistor in a TO-39 metal package.
 NPN complements: BSS51 and BSS52.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector, connected to case

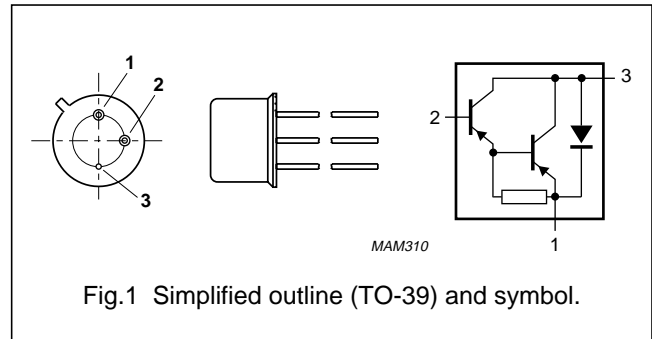


Fig.1 Simplified outline (TO-39) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter				
	BSS61		–	–	–80	V
	BSS62		–	–	–90	V
V_{CES}	collector-emitter voltage	$V_{BE} = 0$				
	BSS61		–	–	–60	V
	BSS62		–	–	–80	V
I_C	collector current (DC)		–	–	–1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$	–	–	0.8	W
		$T_{case} \leq 25\text{ }^\circ\text{C}$	–	–	5	W
h_{FE}	DC current gain	$I_C = -500\text{ mA}; V_{CE} = -10\text{ V}$	2000	–	–	
f_T	transition frequency	$I_C = -500\text{ mA}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}$	–	200	–	MHz

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter			
	BSS61		–	–80	V
	BSS62		–	–90	V
V _{CES}	collector-emitter voltage	V _{BE} = 0			
	BSS61		–	–60	V
	BSS62		–	–80	V
V _{EBO}	emitter-base voltage	open collector	–	–5	V
I _C	collector current (DC)		–	–1	A
I _{CM}	peak collector current		–	–2	A
I _B	base current (DC)		–	–100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	–	0.8	W
		T _{case} ≤ 25 °C	–	5	W
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	200	°C
T _{amb}	operating ambient temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	in free air	220	K/W
R _{th j-c}	thermal resistance from junction to case		35	K/W

PNP Darlington transistors

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CHARACTERISTICS $T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CES}	collector cut-off current					
	BSS61	$V_{BE} = 0; V_{CE} = -60\text{ V}$	–	–	–50	nA
	BSS62	$V_{BE} = 0; V_{CE} = -80\text{ V}$	–	–	–50	nA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = -4\text{ V}$	–	–	–100	nA
h_{FE}	DC current gain	$I_C = -150\text{ mA}; V_{CE} = -10\text{ V}$	1000	–	–	
		$I_C = -500\text{ mA}; V_{CE} = -10\text{ V}$	2000	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -0.5\text{ mA}$	–	–	–1.3	V
		$I_C = -500\text{ mA}; I_B = -0.5\text{ mA}; T_j = 200\text{ °C}$	–	–	–1.3	V
V_{CEsat}	collector-emitter saturation voltage	BSS61				
		$I_C = -1\text{ A}; I_B = -1\text{ mA}$	–	–	–1.6	V
		$I_C = -1\text{ A}; I_B = -1\text{ mA}; T_j = 200\text{ °C}$	–	–	–1.6	V
V_{CEsat}	collector-emitter saturation voltage	BSS62				
		$I_C = -1\text{ A}; I_B = -4\text{ mA}$	–	–	–1.6	V
		$I_C = -1\text{ A}; I_B = -4\text{ mA}; T_j = 200\text{ °C}$	–	–	–1.6	V
V_{BEsat}	base-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -0.5\text{ mA}$	–	–	–1.9	V
V_{BEsat}	base-emitter saturation voltage	BSS61				
		$I_C = -1\text{ A}; I_B = -1\text{ mA}$	–	–	–2.2	V
		BSS62				
		$I_C = -1\text{ A}; I_B = -4\text{ mA}$	–	–	–2.2	V
f_T	transition frequency	$I_C = -500\text{ mA}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}$	–	200	–	MHz
Switching times (between 10% and 90% levels)						
t_{on}	turn-on time	$I_{Con} = -500\text{ mA}; I_{Bon} = -0.5\text{ mA}; I_{Boff} = 0.5\text{ mA}$	–	0.5	–	μs
		$I_{Con} = -1\text{ A}; I_{Bon} = -1\text{ mA}; I_{Boff} = 1\text{ mA}$	–	0.4	–	μs
t_{off}	turn-off time	$I_{Con} = -500\text{ mA}; I_{Bon} = -0.5\text{ mA}; I_{Boff} = 0.5\text{ mA}$	–	0.7	–	μs
		$I_{Con} = -1\text{ A}; I_{Bon} = -1\text{ mA}; I_{Boff} = 1\text{ mA}$	–	1.5	–	μs

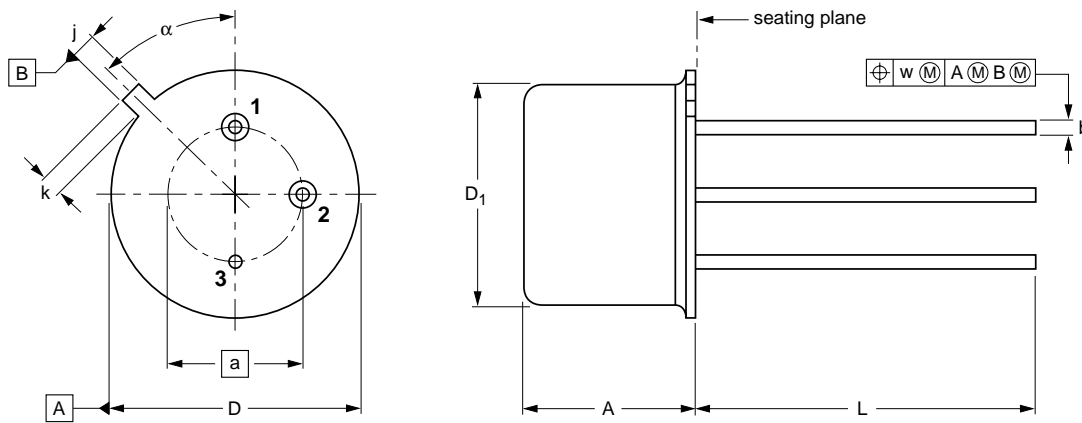
PNP Darlington transistors

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PACKAGE OUTLINE

Metal-can cylindrical single-ended package; 3 leads

SOT5/11



DIMENSIONS (mm are the original dimensions)

UNIT	A	a	b	D	D ₁	j	k	L	w	α
mm	6.60 6.35	5.08	0.48 0.41	9.39 9.08	8.33 8.18	0.85 0.75	0.95 0.75	14.2 12.7	0.2	45°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT5/11		TO-39				97-04-11

PNP Darlington transistors

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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PNP Darlington transistors

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