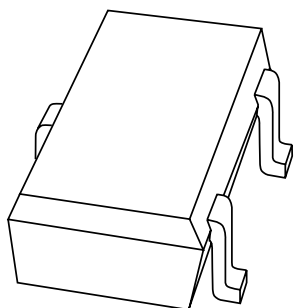


DATA SHEET



PMST4403 PNP switching transistor

Product specification
Supersedes data of August 1993
File under Discrete Semiconductors, SC04

1997 May 29

PNP switching transistor

PMST4403

FEATURES

- High current (max. 600 mA)
- Low voltage (max. 40 V).

APPLICATIONS

- Switching and linear amplification.

DESCRIPTION

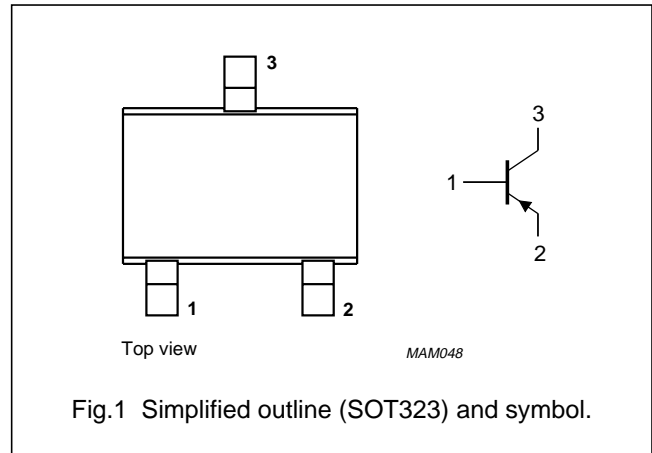
PNP switching transistor in a SOT323 plastic package.
NPN complement: PMST4401.

MARKING

TYPE NUMBER	MARKING CODE
PMST4403	t2T

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–40	V
V_{CEO}	collector-emitter voltage	open base	–	–40	V
I_C	collector current (DC)		–	–600	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	–	200	mW
h_{FE}	DC current gain	$I_C = -150\text{ mA}; V_{CE} = -2\text{ V}$	100	300	
f_T	transition frequency	$I_C = -20\text{ mA}; V_{CE} = -10\text{ V}; f = 100\text{ MHz}$	200	–	MHz
t_{off}	turn-off time	$I_{Con} = -150\text{ mA}; I_{Bon} = -15\text{ mA}; I_{Boff} = 15\text{ mA}$	–	350	ns

PNP switching transistor

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–40	V
V_{CEO}	collector-emitter voltage	open base	–	–40	V
V_{EBO}	emitter-base voltage	open collector	–	–5	V
I_C	collector current (DC)		–	–600	mA
I_{CM}	peak collector current		–	–800	mA
I_{BM}	peak base current		–	–200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	625	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

PNP switching transistor

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CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0; V_{CB} = -40\text{ V}$	–	–50	nA
		$I_E = 0; V_{CB} = -40\text{ V}; T_j = 150\text{ }^{\circ}\text{C}$	–	–10	μA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = -5\text{ V}$	–	–50	nA
h_{FE}	DC current gain	$V_{CE} = -1\text{ V}$; see Fig.2	–	–	
		$I_C = -0.1\text{ mA}$	30	–	
		$I_C = -1\text{ mA}$	60	–	
		$I_C = -10\text{ mA}$	100	–	
h_{FE}	DC current gain	$I_C = -150\text{ mA}; V_{CE} = -2\text{ V}$; note 1	100	300	
		$I_C = -500\text{ mA}; V_{CE} = -2\text{ V}$; note 1	20	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -150\text{ mA}; I_B = -15\text{ mA}$; note 1	–	–400	mV
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$; note 1	–	–750	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = -150\text{ mA}; I_B = -15\text{ mA}$; note 1	+750	–950	mV
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$; note 1	–	–1.3	V
C_c	collector capacitance	$I_E = i_e = 0; V_{CB} = -10\text{ V}; f = 1\text{ MHz}$	–	8.5	pF
C_e	emitter capacitance	$I_C = i_c = 0; V_{EB} = -500\text{ mV}; f = 1\text{ MHz}$	–	35	pF
f_T	transition frequency	$I_C = -20\text{ mA}; V_{CE} = -10\text{ V}; f = 100\text{ MHz}$	200	–	MHz
Switching times (between 10% and 90% levels); see Fig.3					
t_{on}	turn-on time	$I_{Con} = -150\text{ mA}; I_{Bon} = -15\text{ mA}; I_{Boff} = 15\text{ mA}$	–	40	ns
t_d	delay time		–	15	ns
t_r	rise time		–	30	ns
t_{off}	turn-off time		–	350	ns
t_s	storage time		–	300	ns
t_f	fall time		–	50	ns

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

PNP switching transistor

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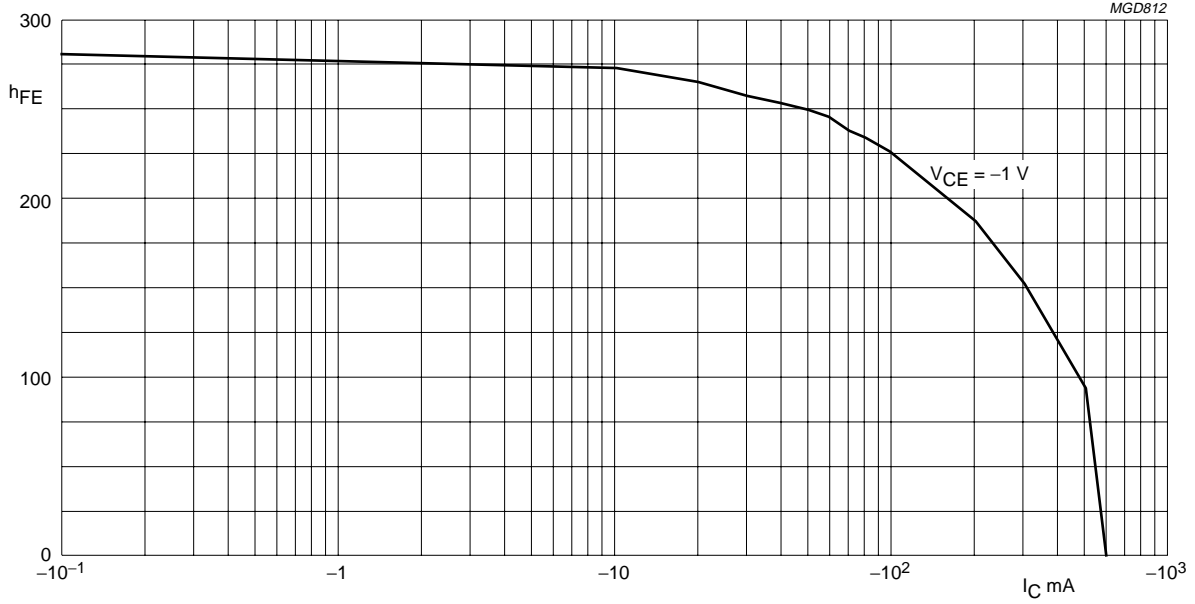
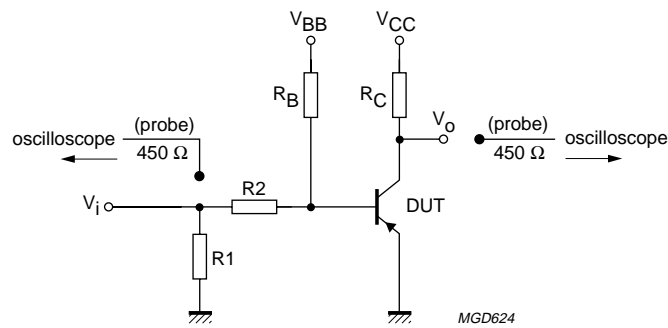


Fig.2 DC current gain; typical values.



$V_i = -9.5 \text{ V}$; $T = 500 \mu\text{s}$; $t_p = 10 \mu\text{s}$; $t_r = t_f \leq 3 \text{ ns}$.
 $R_1 = 68 \Omega$; $R_2 = 325 \Omega$; $R_B = 325 \Omega$; $R_C = 160 \Omega$.
 $V_{BB} = 3.5 \text{ V}$; $V_{CC} = -29.5 \text{ V}$.
 Oscilloscope input impedance $Z_i = 50 \Omega$.

Fig.3 Test circuit for switching times.

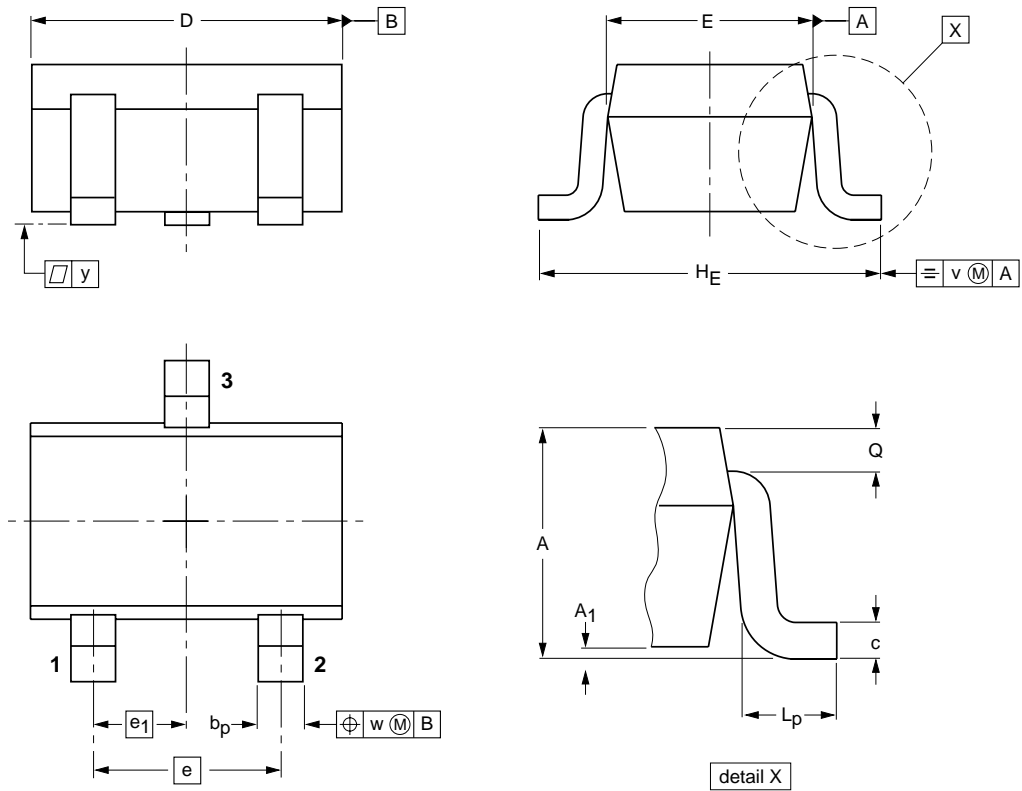
PNP switching transistor

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PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

PNP switching transistor

PMST4403

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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