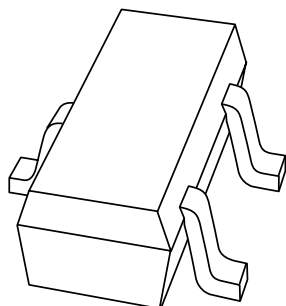


# DATA SHEET



## **PDTTC144EE** NPN resistor-equipped transistor

Preliminary specification  
File under Discrete Semiconductors, SC04

1997 Jul 03

# NPN resistor-equipped transistor

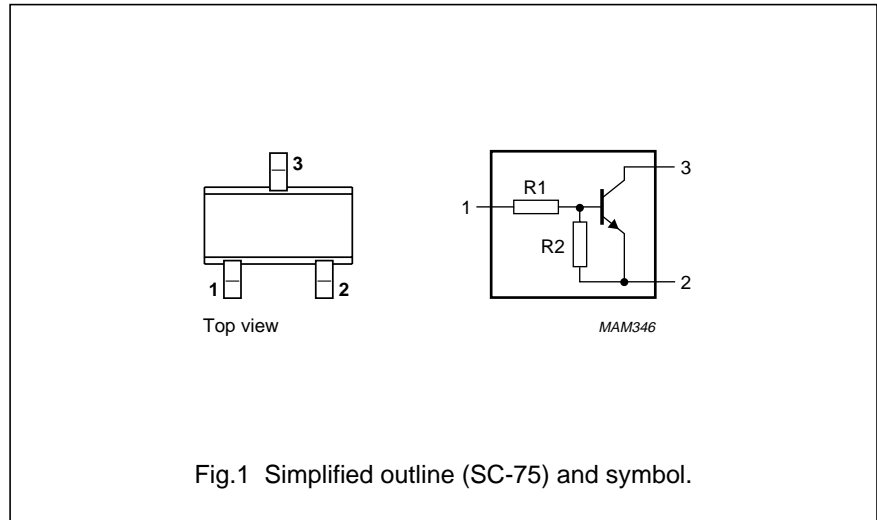
# PDTC144EE

## FEATURES

- Built-in bias resistors R1 and R2 (typ. 47 kΩ each)
- Simplification of circuit design
- Reduces number of components and board space.

## APPLICATIONS

- Especially suitable for space reduction in interface and driver circuits
- Inverter circuit configurations without use of external resistors.

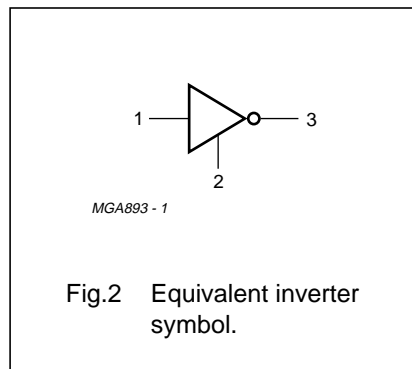


## DESCRIPTION

NPN resistor-equipped transistor in an SC-75 plastic package.  
PNP complement: PDTA144EE.

## PINNING

| PIN | DESCRIPTION      |
|-----|------------------|
| 1   | base/input       |
| 2   | emitter/ground   |
| 3   | collector/output |



## MARKING

| TYPE NUMBER | MARKING CODE |
|-------------|--------------|
| PDTC144EE   | 08           |

## QUICK REFERENCE DATA

| SYMBOL          | PARAMETER                 | CONDITIONS                               | MIN. | TYP. | MAX. | UNIT |
|-----------------|---------------------------|--|------|------|------|------|
| $V_{CE0}$       | collector-emitter voltage | open base                                | –    | –    | 50   | V    |
| $I_O$           | output current (DC)       |  | –    | –    | 100  | mA   |
| $I_{CM}$        | peak collector current    |  | –    | –    | 100  | mA   |
| $P_{tot}$       | total power dissipation   | $T_{amb} \leq 25\text{ °C}$              | –    | –    | 150  | mW   |
| $h_{FE}$        | DC current gain           | $I_C = 5\text{ mA}; V_{CE} = 5\text{ V}$ | 68   | –    | –    |      |
| R1              | input resistor            |  | 33   | 47   | 61   | kΩ   |
| $\frac{R2}{R1}$ | resistor ratio            |  | 0.8  | 1    | 1.2  |      |

## NPN resistor-equipped transistor

## PDTC144EE

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL    | PARAMETER                             | CONDITIONS                           | MIN. | MAX. | UNIT |
|-----------|---------------------------------------|--------------------------------------|------|------|------|
| $V_{CBO}$ | collector-base voltage                | open emitter                         | –    | 50   | V    |
| $V_{CEO}$ | collector-emitter voltage             | open base                            | –    | 50   | V    |
| $V_{EBO}$ | emitter-base voltage                  | open collector                       | –    | 10   | V    |
| $V_I$     | input voltage<br>positive<br>negative |                                      | –    | +40  | V    |
|           |                                       |                                      | –    | –10  | V    |
| $I_O$     | output current (DC)                   |                                      | –    | 100  | mA   |
| $I_{CM}$  | peak collector current                |                                      | –    | 100  | mA   |
| $P_{tot}$ | total power dissipation               | $T_{amb} \leq 25\text{ °C}$ ; note 1 | –    | 150  | mW   |
| $T_{stg}$ | storage temperature                   |                                      | –65  | +150 | °C   |
| $T_j$     | junction temperature                  |                                      | –    | 150  | °C   |
| $T_{amb}$ | operating ambient temperature         |                                      | –65  | +150 | °C   |

**Note**

1. Transistor mounted on an FR4 printed-circuit board.

**THERMAL CHARACTERISTICS**

| SYMBOL        | PARAMETER                                   | CONDITIONS | VALUE | UNIT |
|---------------|---|------------|-------|------|
| $R_{th\ j-a}$ | thermal resistance from junction to ambient | note 1     | 833   | K/W  |

**Note**

1. Transistor mounted on an FR4 printed-circuit board.

**CHARACTERISTICS**

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

| SYMBOL            | PARAMETER                            | CONDITIONS  | MIN. | TYP. | MAX. | UNIT          |
|-------------------|--------------------------------------|---|------|------|------|---------------|
| $I_{CBO}$         | collector cut-off current            | $I_E = 0$ ; $V_{CB} = 50\text{ V}$                            | –    | –    | 100  | nA            |
| $I_{CEO}$         | collector cut-off current            | $I_B = 0$ ; $V_{CE} = 30\text{ V}$                            | –    | –    | 1    | $\mu\text{A}$ |
|                   |                                      | $I_B = 0$ ; $V_{CE} = 30\text{ V}$ ; $T_j = 150\text{ °C}$    | –    | –    | 50   | $\mu\text{A}$ |
| $I_{EBO}$         | emitter cut-off current              | $I_C = 0$ ; $V_{EB} = 5\text{ V}$                             | –    | –    | 500  | $\mu\text{A}$ |
| $h_{FE}$          | DC current gain                      | $I_C = 5\text{ mA}$ ; $V_{CE} = 5\text{ V}$                   | 68   | –    | –    |               |
| $V_{CEsat}$       | collector-emitter saturation voltage | $I_C = 10\text{ mA}$ ; $I_B = 0.5\text{ mA}$                  | –    | –    | 300  | mV            |
| $V_{i(off)}$      | input-off voltage                    | $I_C = 100\text{ }\mu\text{A}$ ; $V_{CE} = 5\text{ V}$        | –    | –    | 500  | mV            |
| $V_{i(on)}$       | input-on voltage                     | $I_C = 2\text{ mA}$ ; $V_{CE} = 300\text{ mV}$                | 3    | –    | –    | V             |
| $R_1$             | input resistor                       |   | 33   | 47   | 61   | k $\Omega$    |
| $\frac{R_2}{R_1}$ | resistor ratio                       |   | 0.8  | 1    | 1.2  |               |
| $C_c$             | collector capacitance                | $I_E = I_B = 0$ ; $V_{CB} = 10\text{ V}$ ; $f = 1\text{ MHz}$ | –    | –    | 3.5  | pF            |

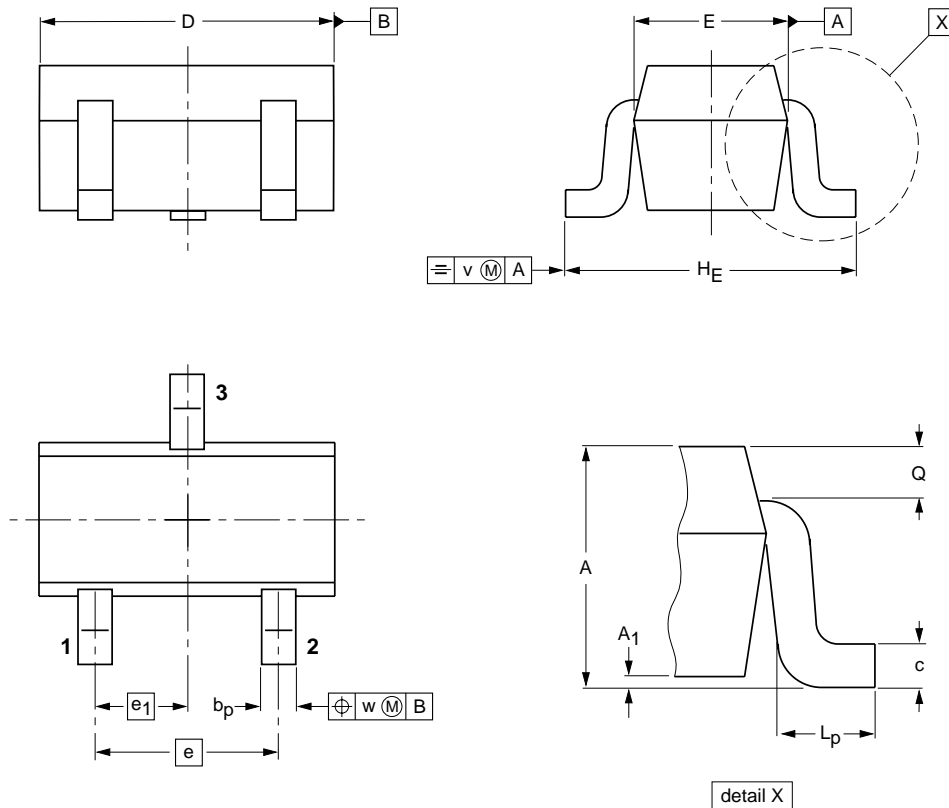
# NPN resistor-equipped transistor

# PDTC144EE

## PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT416



DIMENSIONS (mm are the original dimensions)

| UNIT | A            | A <sub>1</sub><br>max | b <sub>p</sub> | c            | D          | E          | e | e <sub>1</sub> | H <sub>E</sub> | L <sub>p</sub> | Q            | v   | w   |
|------|--------------|-----------------------|----------------|--------------|------------|------------|---|----------------|----------------|----------------|--------------|-----|-----|
| mm   | 0.95<br>0.60 | 0.1                   | 0.30<br>0.15   | 0.25<br>0.10 | 1.8<br>1.4 | 0.9<br>0.7 | 1 | 0.5            | 1.75<br>1.45   | 0.45<br>0.15   | 0.23<br>0.13 | 0.2 | 0.2 |

| OUTLINE<br>VERSION | REFERENCES |       |       |  | EUROPEAN<br>PROJECTION | ISSUE DATE |
|--------------------|------------|-------|-------|--|------------------------|------------|
|                    | IEC        | JEDEC | EIAJ  |  |                        |            |
| SOT416             |            |       | SC-75 |  |                        | 97-02-28   |

## NPN resistor-equipped transistor

PDTC144EE

**DEFINITIONS**

| <b>Data sheet status</b>  |   |
|---|---|
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>  |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>  |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

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NPN resistor-equipped transistor

PDTC144EE

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**NOTES**

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NPN resistor-equipped transistor

PDTC144EE

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**NOTES**

# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

**Belgium:** see The Netherlands

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**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 689 211, Fax. +359 2 689 102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
Tel. +45 32 88 2636, Fax. +45 31 57 0044

**Finland:** Sinikallontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615800, Fax. +358 9 61580920

**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.  
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

**Indonesia:** see Singapore

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,  
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,  
Tel. +48 22 612 2831, Fax. +48 22 612 2327

**Portugal:** see Spain

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2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
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**South America:** Rua do Rocio 220, 5th floor, Suite 51,  
04552-903 São Paulo, SÃO PAULO - SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 829 1849

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 3 301 6312, Fax. +34 3 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 632 2000, Fax. +46 8 632 2745

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**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

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**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 625 344, Fax. +381 11 635 777

**For all other countries apply to:** Philips Semiconductors, Marketing & Sales Communications,  
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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Printed in The Netherlands

117047/00/01/pp8

Date of release: 1997 Jul 03

Document order number: 9397 750 02193

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