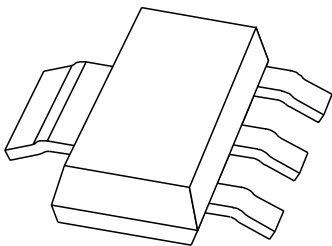


# DATA SHEET



## **BDP32** PNP medium power transistor

Product specification  
Supersedes data of September 1994  
File under Discrete Semiconductors, SC04

1997 Mar 10

## PNP medium power transistor

BDP32

## FEATURES

- High current (max. 3 A)
- Low voltage (max. 45 V).

## APPLICATIONS

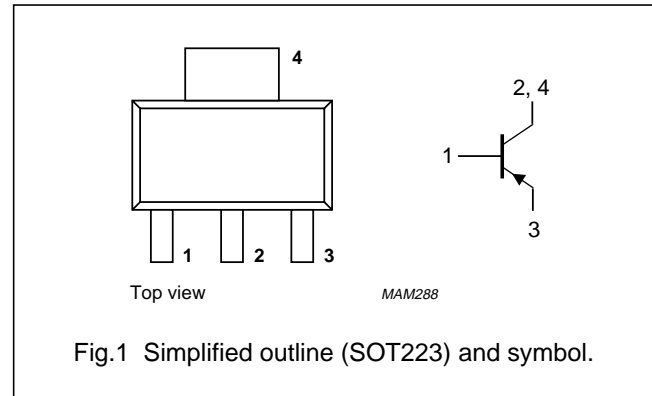
- General purpose medium power applications.

## DESCRIPTION

PNP medium power transistor in a SOT223 plastic package. NPN complement: BDP31.

## PINNING

PIN	DESCRIPTION
1	base
2,4	collector
3	emitter



## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–45	V
$V_{CEO}$	collector-emitter voltage	open base	–	–45	V
$I_{CM}$	peak collector current		–	–6	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ }^{\circ}\text{C}$	–	1.35	W
$h_{FE}$	DC current gain	$I_C = -500\text{ mA}; V_{CE} = -12\text{ V}$	40	–	
$f_T$	transition frequency	$I_C = -250\text{ mA}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}$	60	–	MHz

## PNP medium power transistor

BDP32

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–45	V
$V_{CEO}$	collector-emitter voltage	open base	–	–45	V
$V_{EBO}$	emitter-base voltage	open collector	–	–5	V
$I_C$	collector current (DC)		–	–3	A
$I_{CM}$	peak collector current		–	–6	A
$I_{BM}$	peak base current		–	–0.5	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 1	–	1.35	W
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	operating ambient temperature		–65	+150	°C

**Note**

1. Device mounted on a printed-circuit board, single sided copper, tinplated, mounting pad for collector 1 cm<sup>2</sup>.  
For other mounting conditions, see “*Thermal considerations for the SOT223 in the General part of handbook SC04*”.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	91	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point		10	K/W

**Note**

1. Device mounted on a printed-circuit board, single sided copper, tinplated, mounting pad for collector 1 cm<sup>2</sup>.  
For other mounting conditions, see “*Thermal considerations for the SOT223 in the General part of handbook SC04*”.

PNP medium power transistor

BDP32

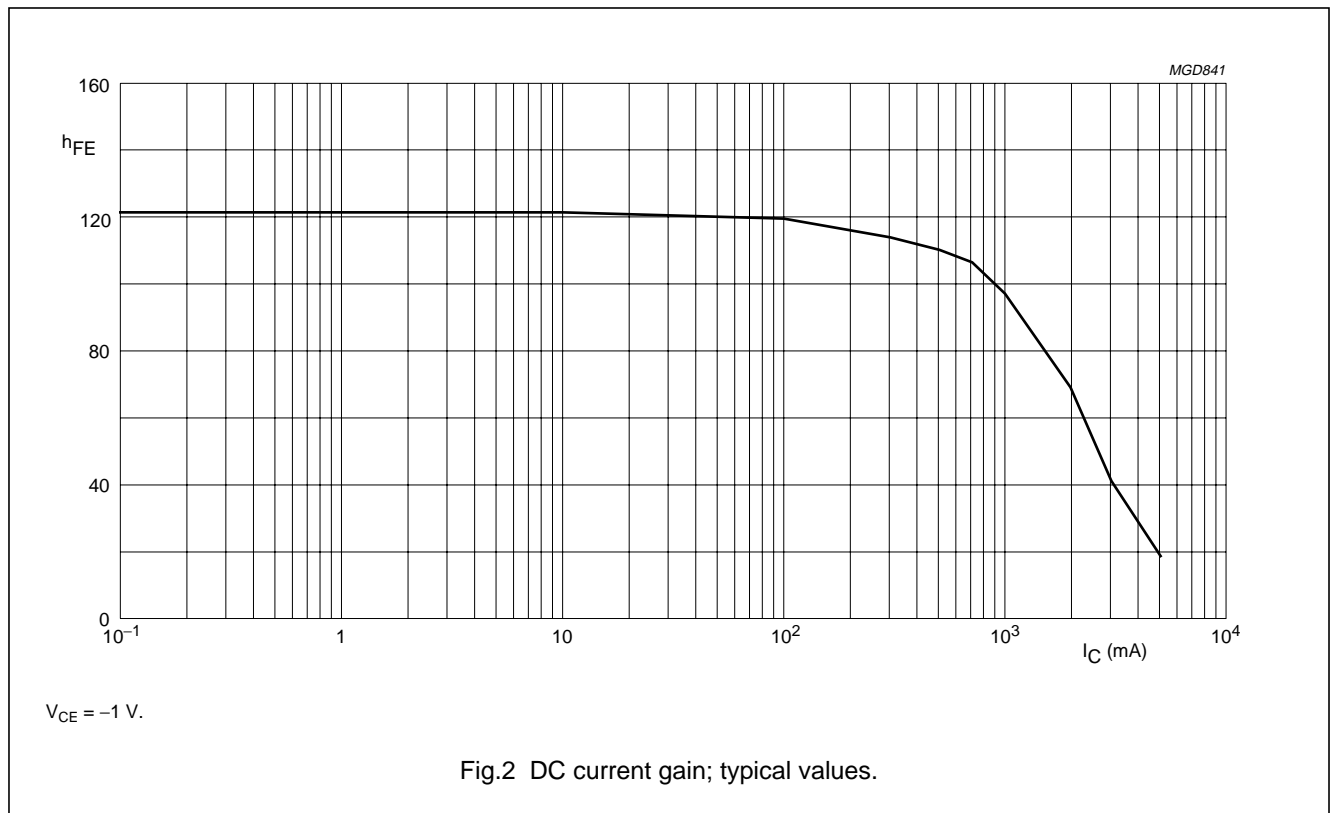
**CHARACTERISTICS**

T<sub>amb</sub> = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I <sub>CBO</sub>	collector cut-off current	I <sub>E</sub> = 0; V <sub>CB</sub> = -40 V	-	-50	nA
		I <sub>E</sub> = 0; V <sub>CB</sub> = -40 V; T <sub>j</sub> = 150 °C	-	-10	µA
I <sub>EBO</sub>	emitter cut-off current	I <sub>C</sub> = 0; V <sub>EB</sub> = -5 V	-	-50	nA
h <sub>FE</sub>	DC current gain	I <sub>C</sub> = -0.5 A; V <sub>CE</sub> = -12 V; note 1; see Fig.2	40	-	
		I <sub>C</sub> = -2 A; V <sub>CE</sub> = -1 V; note 1; see Fig.2	20	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = -500 mA; I <sub>B</sub> = -50 mA; note 1	-	-300	mV
		I <sub>C</sub> = -2 A; I <sub>B</sub> = -200 mA; note 1	-	-700	mV
V <sub>BEsat</sub>	base-emitter saturation voltage	I <sub>C</sub> = -500 mA; I <sub>B</sub> = -50 mA; note 1	-	-1.2	V
		I <sub>C</sub> = -2 A; I <sub>B</sub> = -200 mA; note 1	-	-1.5	V
f <sub>T</sub>	transition frequency	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -250 mA; f = 100 MHz	60	-	MHz

**Note**

1. Pulse test: t<sub>p</sub> ≤ 300 µs; δ ≤ 0.02.



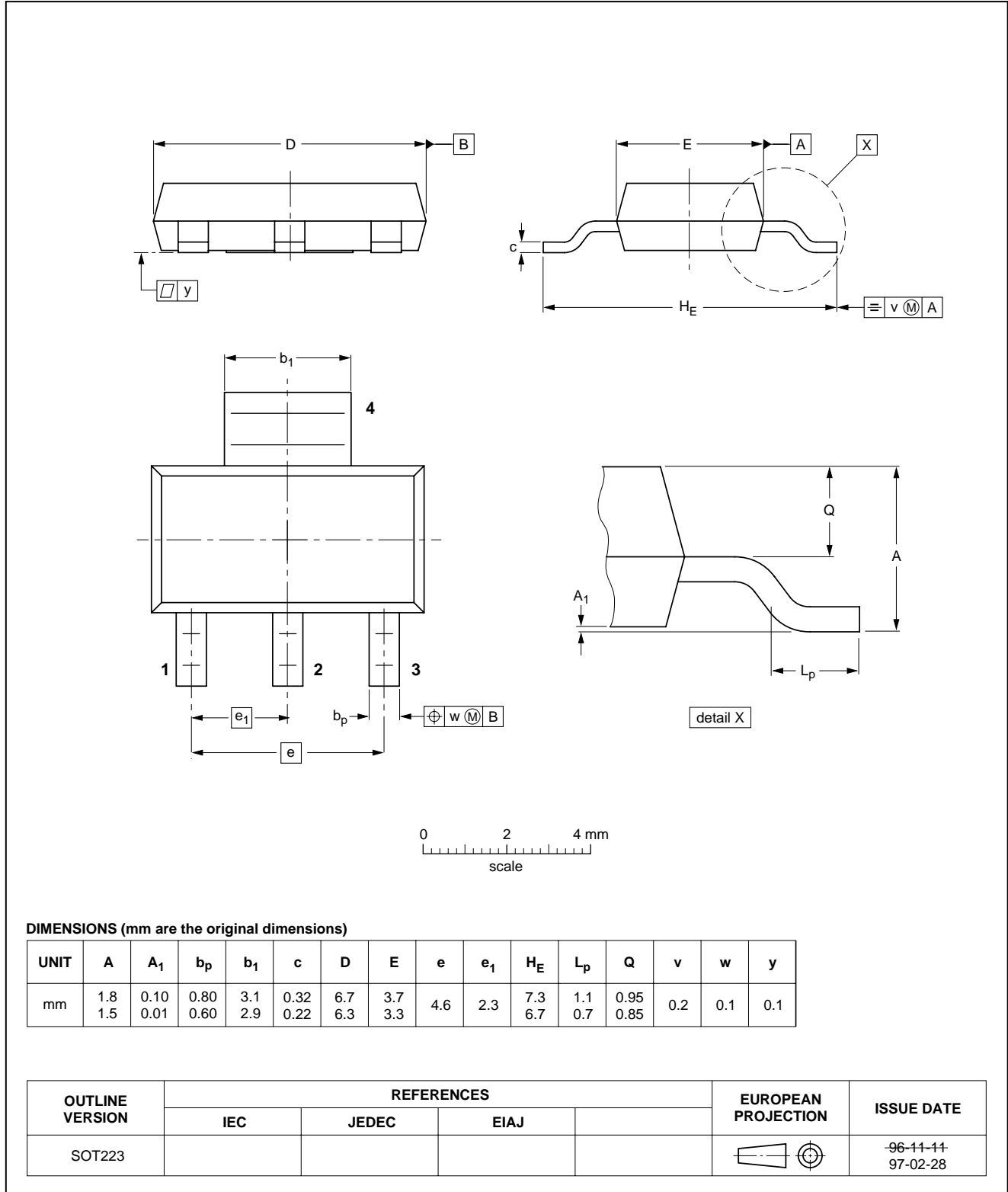
# PNP medium power transistor

BDP32

## PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



## PNP medium power transistor

BDP32

**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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PNP medium power transistor

BDP32

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