Optimized Reconfigurable Cell Array (ORCA™)
OR3Cxxx/OR3Txxx Series Field-Programmable Gate Arrays

Features

- High-performance, cost-effective 0.35 μm, 4-level metal technology, with a migration plan for 0.25 μm technology (four-input look-up table delay less than 1.7 ns with -5 speed grade in 0.35 μm).
- Up to 125,000 usable gates in 0.35 μm, expanding to 225,000 usable gates in 0.25 μm.
- Up to 448 user I/Os in 0.35 μm. (OR3Txxx I/Os are 5 V tolerant to allow interconnection to both 3.3 V and 5 V devices, selectable on a per-pin basis.)
- Twin-quad PFU architecture with eight 16-bit look-up tables (LUTs) per PFU, organized in two nibbles for use in nibble- or byte-wide functions. Allows for mixed arithmetic and logic functions in a single PFU.
- Nine user flip-flops per PFU, one following each LUT, plus one extra. All have programmable clock enable and local set/reset plus a global set/reset that can be disabled per PFU.
- New Flexible INput Structure (FINS) of the PFUs provides the routability enhancement of shared input LUTs and the logic flexibility of independent LUT inputs.
- Internal fast-carry for nibble- or byte-wide arithmetic functions, with option to register carry-out for either.
- New soft-wired LUTs allow fast cascading of up to three levels of LUT logic in a single PFU without using local PFU routing resources.
- Synthesis friendly by design.
- New supplemental logic and interconnect cell (SLIC) provides 3-statable buffers, up to 10-bit decoder, and PAL*-like AND-OR-Invert (AOI) in each PLC.
- Abundant hierarchical routing resources, based on routing two data nibbles and two control lines per set, provides for faster place and route implementations and less routing delay.
- TTL or CMOS input levels are programmable per pin for the OR3Cxxx (5 V) devices.
- Individually programmable drive capability: 24 mA sink/12 mA source, 12 mA sink/6 mA source, or 6 mA sink/3 mA source.
- Built-in boundary scan (IEEE† 1149.1).
- Enhanced system clock routing for low-skew, high-speed clocks originating on-chip or at any I/O.
- Up to four new ExpressCLK inputs allow extremely fast clocking of signals on- and off-chip with access to general clock routing.
- New clock stop circuitry to glitchlessly stop and start the ExpressCLKs independently by user command.
- New programmable I/O cell (PIC) input has:
  — Fast-capture latch and input FF/latch for reduced input setup time and zero hold time.
  — Capability to demultiplex input signals.
  — Fast access to SLIC for decodes and PAL-like functions.
- New programmable I/O cell output has:
  — Fast-output register with signal multiplexing capability.
  — Two-input function capability.
  — Fast open-drain drive capability.

Table 1. Lucent Technologies’ ORCA OR3Cxxx/OR3Txxx Series FPGAs

<table>
<thead>
<tr>
<th>Device</th>
<th>Usable Gates‡</th>
<th>Registers</th>
<th>Max. User RAM</th>
<th>User I/Os</th>
<th>Array Size</th>
<th>Process Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>OR3C/3T30</td>
<td>19K—44K</td>
<td>2212</td>
<td>25K</td>
<td>224</td>
<td>14 x 14</td>
<td>0.35 μm/4 LM</td>
</tr>
<tr>
<td>OR3C/3T55</td>
<td>32K—72K</td>
<td>3492</td>
<td>41K</td>
<td>288</td>
<td>18 x 18</td>
<td>0.35 μm/4 LM</td>
</tr>
<tr>
<td>OR3C/3T80</td>
<td>47K—108K</td>
<td>5060</td>
<td>62K</td>
<td>352</td>
<td>22 x 22</td>
<td>0.35 μm/4 LM</td>
</tr>
<tr>
<td>OR3C/3T125</td>
<td>76K—174K</td>
<td>7952</td>
<td>100K</td>
<td>448</td>
<td>28 x 28</td>
<td>0.35 μm/4 LM</td>
</tr>
<tr>
<td>OR3T165</td>
<td>100K—227K</td>
<td>10240</td>
<td>131K</td>
<td>512</td>
<td>32 x 32</td>
<td>0.25 μm/4 LM</td>
</tr>
<tr>
<td>OR3T225</td>
<td>140K—320K</td>
<td>14212</td>
<td>185K</td>
<td>608</td>
<td>38 x 38</td>
<td>0.25 μm/4 LM</td>
</tr>
</tbody>
</table>

‡ The first number in the usable gates column assumes 96 gates per PFU (12 gates per 4-input LUT/FF pair) for logic-only designs. The second number assumes 30% of a design is RAM. PFUs used as RAM are counted at 4 gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU.

* PAL is a trademark of Advanced Micro Devices, Inc.
† IEEE is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
System-Level Features

System-level features reduce glue logic requirements and make a “system on a chip” possible.

- Full PCI compliance.
- New dual-use microprocessor interface can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA. Glueless interface to i960*, PowerPC, and MC68xxx† processors with user-configurable address space provided.
- New parallel readback capability with the built-in microprocessor interface.
- New programmable clock manager (PCM) adjusts clock phase and duty cycle for input clock rates from 10 MHz to 80 MHz. The PCM may be combined with FPGA logic to create complex functions, such as digital phase-locked loops (DPLL), frequency counters, and frequency synthesizers or clock doublers.
- True internal 3-state, bidirectional buses with simple control provided by the new SLIC.
- 32 x 4 RAM per PFU, configurable as single- or dual-port at >100 MHz. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using new SLIC decoders and bank drivers.

Support

- ORCA Foundry Development System support.
- Supported by industry-standard CAE tools for design entry, synthesis, simulation, and timing analysis.

* i960 is a trademark of Intel Corporation.
† MC68xxx is a trademark of Motorola, Inc.

Description

The ORCA OR3Cxxx/OR3Txxx Series FPGAs consist of three basic elements: programmable logic cells (PLCs), programmable input/output cells (PICs), and system-level features. An array of PLCs is surrounded by PICs. Each PLC contains a programmable function unit (PFU), a SLIC, local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU (see Figure 1), whereas decoders, PAL-like functions, and 3-state buffering can be performed in the SLIC (see Figure 2). The PICs can be used to register signals, perform input demultiplexing, and perform output multiplexing and other functions on two output signals (Figure 3). Some of the system-level functions include the new microprocessor interface and the programmable clock manager (PCM).

Each PFU contains eight 4-input (16-bit) look-up tables (LUTs), eight latches/flip-flops (FFs), and one additional flip-flop. LUTs may be used individually, be combined to produce 5-input LUTs, or be cascaded in a variety of ways to achieve complex functions of up to 21 inputs using the new soft-wired LUT connections.

The PFU is organized in a twin-quad fashion: two sets of four LUTs and FFs, which can be controlled independently. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth FF for pipelining. Each PFU may also be configured as a synchronous 32 x 4 single- or dual-port RAM or ROM. The FFs (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The FFs also have programmable clock polarity, clock enables, and local set/reset.
Description (continued)

Note: LSR can be disabled on a per-nibble basis, and GSR can be disabled per PFU.

Figure 1. Simplified OR3Cxxx/OR3Txxx PFU Diagram
Description (continued)

Figure 2. OR3Cxxx/OR3Txxx SLIC
The SLIC is connected to PLC routing resources and the outputs of the PFU. It contains 3-state, bidirectional buffers and logic to perform up to a 10-bit AND function for decoding, or an AND-OR-INVERT to perform PAL-like functions. The 3-state drivers in the SLIC and their direct connections to the PFU outputs make fast, true 3-state buses possible within the FPGA, reducing required routing and allowing for real-world system performance.

The OR3Cxxx/OR3Txxx PIC addresses the demand for ever-increasing system clock speeds. On the input side, each PIC contains a fast capture latch that is clocked by an ExpressCLK. This latch is followed by a latch/FF that is clocked by a system clock. The combination provides for very low setup requirements and zero hold times for signals coming on-chip. It may also be used to demultiplex an input signal, such as a multiplexed address/data signal, and register the signals without explicitly building a demultiplexer.
Description (continued)

Two input signals are available to the PLC array from each pad, and the ORCA 2C/2T capability to use any input as a clock or other global input is maintained. On the output side of each PIC, two outputs from the PLC array can be routed to each output flip-flop and logic can be associated with each I/O pad. The output logic associated with each pad allows for multiplexing of output signals and other functions of two output signals. The output flip-flop in combination with output signal multiplexing is particularly useful for registering address signals to be multiplexed with data, allowing a full clock cycle for the data to propagate to the output. The I/O buffer associated with each pad is very similar to the ORCA 2C/2T Series buffer with enhanced 24 mA sink/12 mA source capability and a new fast open-drain option for ease of use on system buses.

The abundant routing resources of the OR3Cxxx/OR3Txxx FPGAs is organized to route signals individually or as buses with related control signals. Clocks are routed on a low-skew, high-speed distribution network and may be sourced from PLC logic, externally from any I/O pad, or from the very fast ExpressCLK pins. ExpressCLKs may be glitchlessly, and independently, enabled and disabled with a programmable control signal.

The OR3Cxxx/OR3Txxx series also provides system-level functionality by means of its dual-use microprocessor interface and its innovative programmable clock manager. Some of the capabilities of these features are noted in the Features section at the beginning of this product brief. These features will be further explained in application notes available from Lucent Technologies.

The ORCA Foundry Development System is used to process a design from a netlist to a configured FPGA. This system is used to map your design onto the ORCA architecture and then place and route it using ORCA Foundry’s timing-driven tools. The development system also includes interfaces to, and libraries for, other popular CAE tools for design entry, synthesis, simulation, and timing analysis.

The FPGA’s functionality is determined by internal configuration RAM. The FPGA’s internal initialization/configuration circuitry loads the configuration data at powerup or under system control. The RAM is loaded by using one of several configuration modes. The configuration data resides externally in an EEPROM or any other storage media. Serial EEPROMs provide a simple, low pin count method for configuring FPGAs. A new method for configuring the devices is through the microprocessor interface.

Additional Information

Contact your local Lucent Technologies’ representative for additional information regarding the ORCA OR3Cxxx/OR3Txxx FPGA devices.